UNIVAC® SCIENTIFIC GENERAL-PURPOSE COMPUTER SYSTEM

SYSTEM MAINTENANCE

PX 23

FEBRUARY 1957

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

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SYSTEM MAINTENANCE

INTRODUCTION

1. GENERAL

Maintenance procedures described in this volume include preventive and corrective maintenance of mechanical and electrical components. Preventive maintenance is to be performed periodically. It consists of checking the electronic circuits and cleaning and lubricating the mechanical parts of the equipment so that potential sources of failure may be detected and corrected. Corrective maintenance consists in adjustment and replacement of faulty components.

In maintaining the equipment it is necessary to refer frequently to the unit signal diagrams and the schematic diagrams. There is a single schematic diagram for each unit chassis type in the computer; and there is a unit signal diagram for each individual unit chassis used in the equipment. For example, there is a single schematic diagram for the MD Read/Write Amplifier (61400) chassis, but there are 36 unit signal diagrams, because there are 36 of this chassis type used in the MD Storage System. An individual chassis, such as the 61400, is interchangeable with any other chassis with the same unit chassis number.

Because there are many standard circuits used in the unit chassis, a shorthand symbol system has been employed. To understand thoroughly the electronic operation of the chassis components, it is necessary to learn carefully the operation of the basic circuits represented by the shorthand symbols. The shorthand symbol and the electronic representation of each symbol is given in the following paragraphs, along with explanation of the operation of each circuit.

There are two systems of chassis component layout and identification used in the construction of the unit chassis: the unit symbol series system and the coordinate system. The chassis in the 10000, the 30000, and the 60000 cabinets use the symbol series system, and the chassis in the 55000 cabinet and the Magnetic Tape Storage System (70000 cabinet) use the coordinate. The two systems are explained in paragraph 4.

In trouble shooting the computer system, the block diagrams are used to isolate the trouble in a particular section of the system. Then, by using information taken from the block diagrams, it is often possible to go directly to the unit chassis to isolate the trouble. As was explained previously in THEORY OF OPERATION, BASIC COMPUTER, the block diagrams do not show those circuit elements whose function is signal manipulation only. When a circuit being examined on the block diagram is located on the unit signal diagram, it is apparent that this is the case. After the explanation of the unit symbol series system and the coordinate system, the method of using block diagrams with unit signal diagrams is discussed so that it is possible to transfer quickly from the block diagram to the represented circuits on the unit signal diagrams.

Because it is important that the maintenance personnel have a thorough knowledge of the Supervisory Control Panel, a detailed description of this panel is presented. Other sections describe procedures required for manually inserting a program into the computer from the Supervisory Control Panel, the detailed checking and adjustment procedures for each major section of the equipment, the computer programs which are to be used by the maintenance personnel for checking the logical operation of the equipment, and a preventive maintenance schedule.

Also supplied with this book is a separate set of maintenance pamphlets titled "INFORMATION SHEETS FOR NON-REMINGTON RAND ITEMS". These pamphlets describe maintenance procedures for items purchased from other manufacturers, such as the Flexowriter, motor-alternator set, and motorized valve.

2. UNIT SIGNAL DIAGRAMS AND SCHEMATIC DIAGRAMS

The Univac Scientific is constructed with a large number of unit chassis of the 74-pin plug-in type and of the 19-inch relay rack mounting type. Although over 260 plug-in type unit chassis are used in the basic computer, there are only 67 distinct types of unit chassis, because one chassis type may be used more than once where circuit similarities exist. Where more than one of the same type of unit chassis is used, the unit chassis are interchangeable as to their place in the equipment; i.e., chassis of the same type (same unit chassis construction and unit chassis number) may be used for various similar functions. Each of the unit chassis types is identified by a chassis number and, in general, the chassis number indicates in which cabinet the unit chassis is located. The unit chassis is drawn electrically as a schematic diagram with one schematic diagram for each unit chassis type.

To show how the chassis are interconnected within the computer system, unit signal diagrams are provided. Essentially a unit signal diagram is a copy of the schematic diagram of a unit chassis with signal names, input origins, and output destinations on the input and output lines. There is one unit signal diagram for each jack location in the computer system. Where two or more identically constructed unit chassis are employed for different applications (as for the different stages of a register), their unit signal diagrams will be exactly the same schematically, but will differ in signal names, input origins, and output destinations on the input and output lines. Thus each unit signal diagram is a schematic diagram of a unit chassis and, in addition, gives the signal names, and input-output information associated with that particular jack location. Figure 1 shows the jack locations in the 10000 cabinet.

Table 1 lists the volumes of unit-signal diagrams supplied with the basic computer system. The unit signal diagrams for the input-output equipment, such as the Magnetic Tape Storage System, are provided with the instruction book for this equipment.

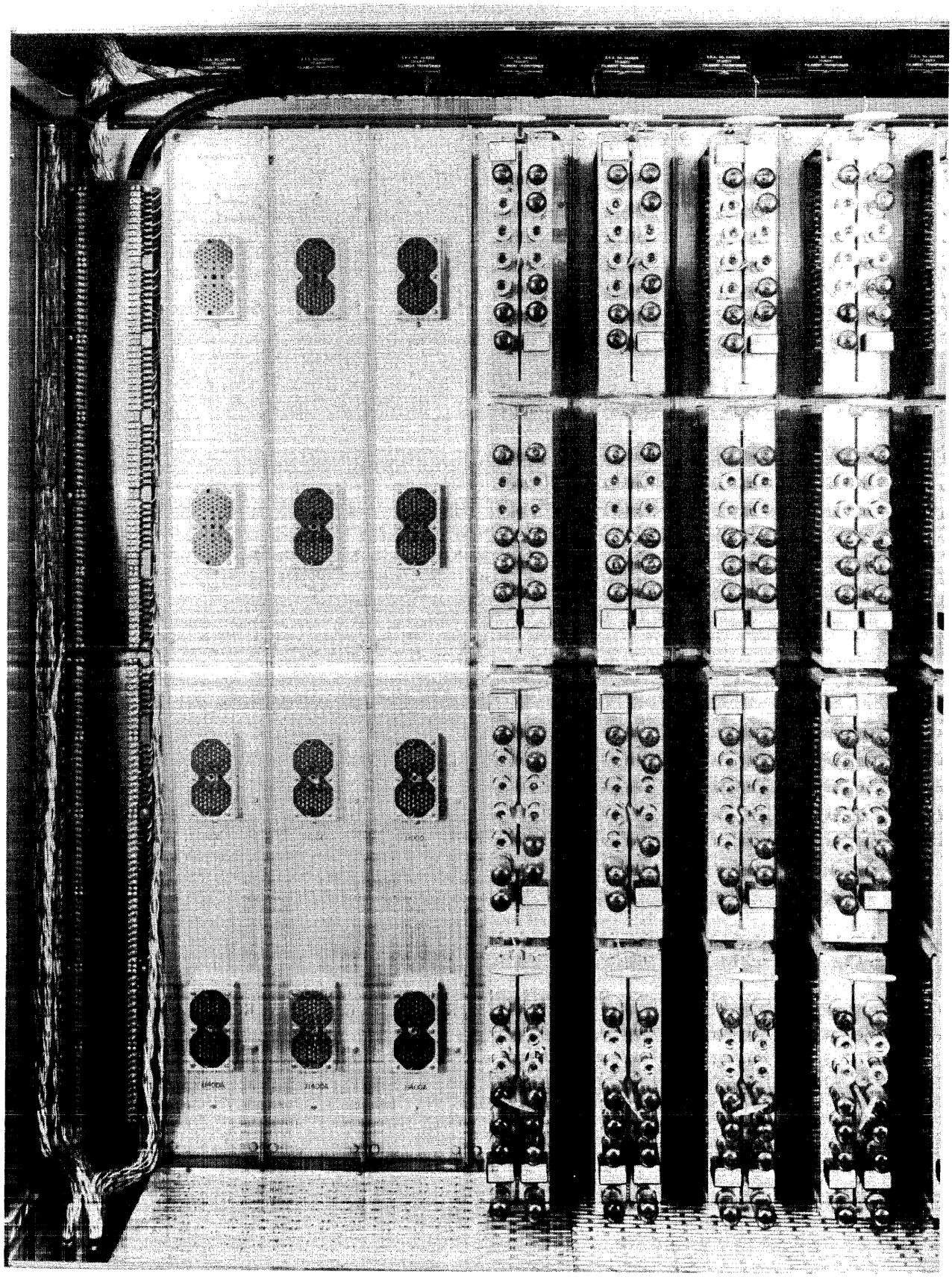


Figure 1. Jack Locations, 10000 Cabinet
PX 131

TABLE 1

LIST OF UNIT SIGNAL DIAGRAMS

Volume	Unit Signal Diagram Sets	Symbol Series
20000 and 40000 cabinets	Operator's Table	
	Relay Panel	26100
	Photoelectric Tape Reader Power Supply	26200
	High Speed Punch	26300
	Typewriter	26400
	Photoelectric Tape Reader	26700
	Supervisory Control Cabinet	
	Supervisory Control Panel	40000
	Address Monitor	41000
10000 cabinet	Arithmetic Cabinet	10000
30000 cabinet	Control Cabinet	30000
55000 cabinet	Magnetic Core Storage Cabinet	55000
60000 cabinet	Magnetic Drum Storage Cabinet	60000
80000 and 90000 cabinets	Main Power Supply	80000
	Motor-Generator Assembly	88000
	Blower Cabinet	90000

3. SHORTHAND SYMBOL SYSTEM

a. GENERAL. - To conserve space on each of the three kinds of diagrams, block-type symbols are used where possible. Unit signal diagrams and schematic diagrams employ special "shorthand symbols" to represent six standard circuits which are used frequently throughout the computer. Block diagrams, on the other hand, are composed entirely of block symbols, and the symbols used on the block diagrams are different from those used on the schematic and unit signal diagrams. Each symbol by its size, shape, inputs, outputs, and other identifying information represents a particular circuit or a particular logical element. The block symbols are explained in detail in the introductory section of THEORY OF OPERATION, BASIC COMPUTER.

The following subparagraphs explain the shorthand symbols used on the unit signal diagrams and the schematic diagrams. Basically, these symbols are standard in both the symbol series system and the coordinate system of chassis construction. In the front of each unit signal diagram volume there is a diagram titled "Shorthand Symbols for Schematic Diagrams" which shows all symbols used in that volume.

b. TUBE ELEMENT CONNECTIONS. - Symbols for the various tube element connections are shown in Figure 2. These symbols are used on all three types of diagrams and should be memorized by maintenance personnel.

c. SHORTHAND SCHEMATIC SYMBOLS. - The specific symbols used on schematic and unit signal diagrams are discussed in the following subparagraphs. If a stage or subcircuit is used repeatedly throughout the equipment, and is identical wherever it appears, it is called a "standard stage". All standard stages of the same type are identical electrically; for example, two standard stage flip-flops receiving identical input signals, theoretically, produce identical outputs. Each of the principal standard stages explained below in detail will be found represented by its respective "shorthand schematic symbol" when it appears on a schematic-type diagram.

The principal standard stages are flip-flops, cathode followers, inverters, gates, amplifiers, and pulse transformers.

(1) FLIP-FLOP. - The Eccles-Jordan trigger circuit, or flip-flop, is a form of multivibrator employing direct coupling between the plates and grids of two tubes. It is essentially a device which provides an output of a steady d-c voltage when correspondingly triggered by a momentary pulse of relatively short duration. This steady d-c output remains until removed by another separate triggering of the flip-flop. For example, in Figure 3, one condition of equilibrium exists if the triode in side "A" of the flip-flop tube is conducting and the triode in side "B" is cut off, and the other condition of equilibrium exists if the triode in side "A" is cut off and side "B" is conducting. Regardless of which of these two states the flip-flop is in, it remains in the current state until some external impulse causes it to reverse its state. After such a reversal, the flip-flop remains in the second state until another external impulse is applied to revert the flip-flop to its first state. The term "flip-flop" is derived from this property of "flopping" from state to state.

Since the circuitry in both halves of the flip-flop is identical, it seems that equal plate current should flow through the triode in each half when plate voltage is applied; however, slight unbalances are always present. This unbalance causes a greater plate current to flow in one of the tube's twin triodes when plate voltage is applied. If the greater plate current flows in the triode in side "A", a proportionally larger voltage drop occurs across plate resistors R83 and R84, in side "B"; therefore, the voltage at the plate of the triode in side "A" is lower than that at the plate of the triode in side "B". The lower plate potential at the triode in side "A" is applied to the grid of the triode in side "B" through the voltage divider consisting of R88 and R92. The decreasing potential at this grid causes a further decrease in the plate current of the triode in side "B". The decrease of current in side "B" causes a corresponding rise in its plate voltage. This rise in plate voltage is applied to the grid of the triode in side "A" through the voltage divider consisting of R87 and R91. These incremental changes continue until a state of equilibrium is reached, at which time the triode in side "B" is cut off and the triode in side "A" fully conducting.

To reverse the state of equilibrium, a negative going pulse is applied through CR80 to the grid of the triode in side A. The decrease in voltage on the grid of this triode causes a drop in its plate current. The drop in plate

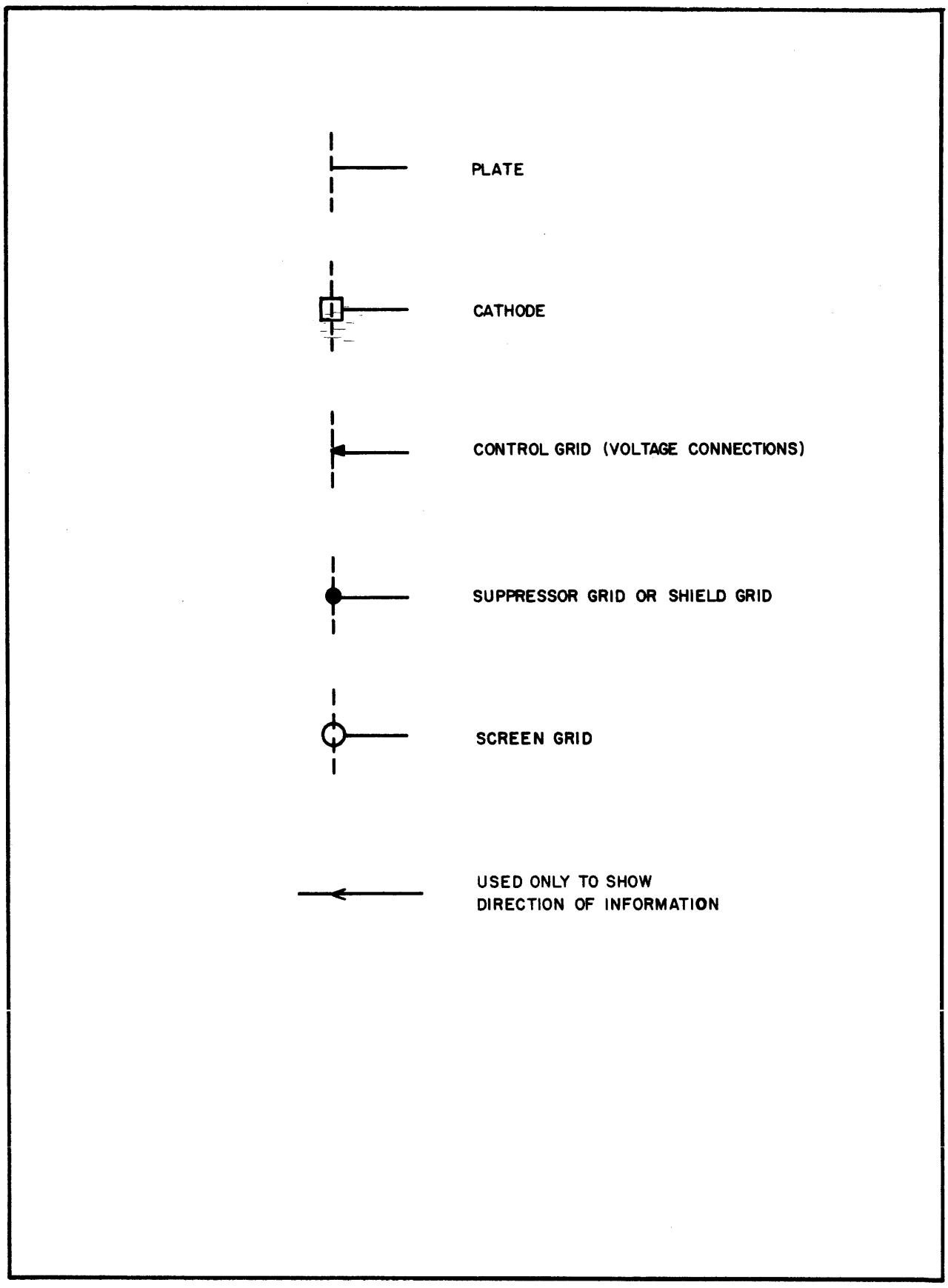


Figure 2. Tube Element Connections.
PX 131

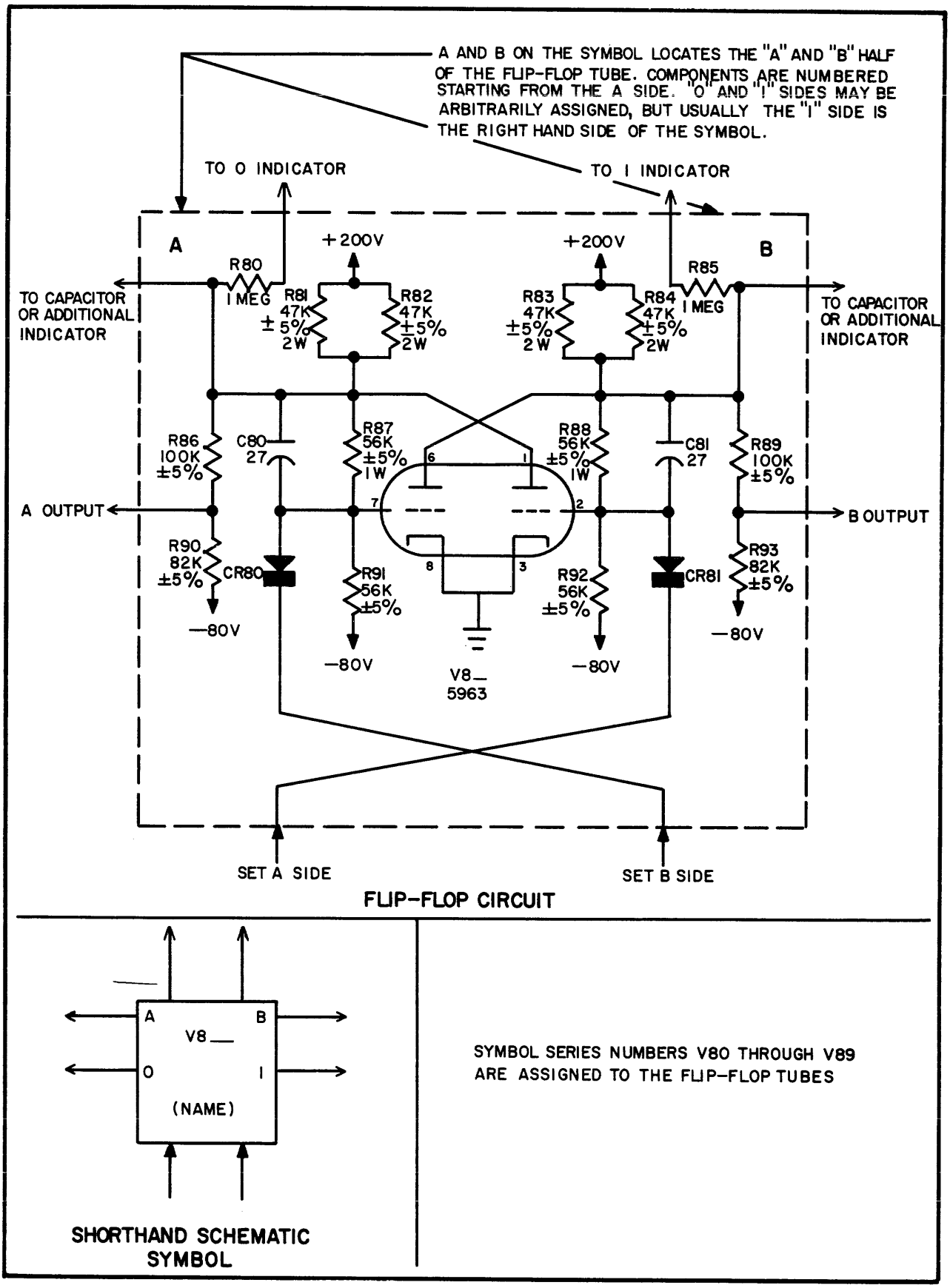


Figure 3. STANDARD Flip-flop Stage
PX 131

current causes a rise in plate voltage, which is applied to the grid of the triode in side B through the voltage divider consisting of R88 and R92. This rise in grid voltage causes the plate of the triode in side B to start to conduct. This triode, when conducting, draws more current and therefore has a lower plate voltage, which is applied to the grid of the triode in side A through the voltage divider consisting of R87 and R91. The reduced voltage at the grid of the triode in side A drives that tube closer to cut-off and the triode in side B to heavier conduction. The process continues until the triode in side A cuts off and that in side B fully conducts. This condition represents the second state of equilibrium.

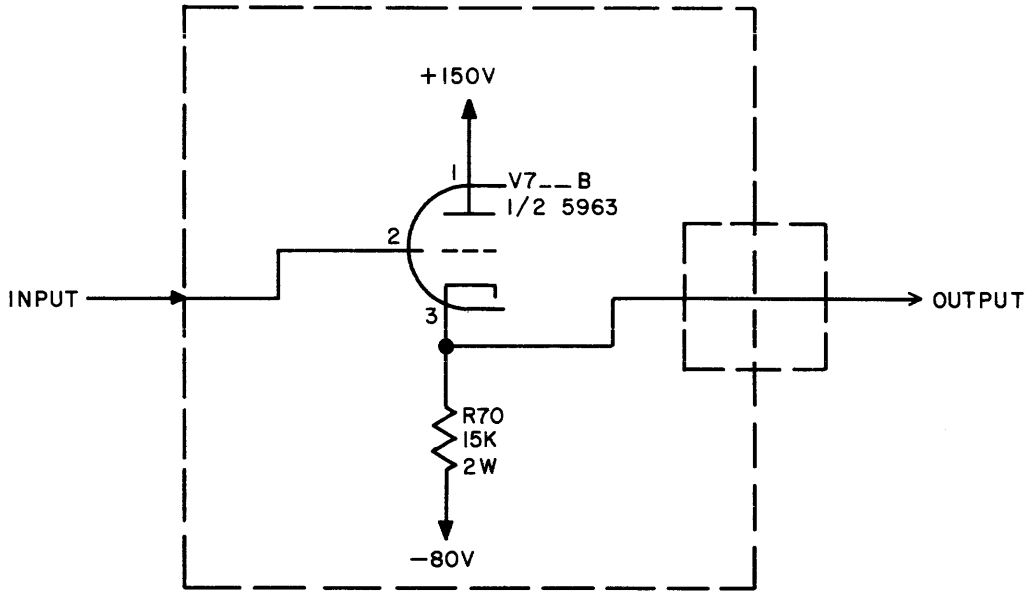
The shorthand schematic symbol for the standard flip-flop stage is also shown in Figure 3. Usually the "A" side of the flip-flop is called the "0" state and the "B" side is called the "1" state. The input line on the "0" side of the flip-flop symbol indicates an input signal to set the flip-flop to "0"; the input line to the "1" side indicates a similar input to set the flip-flop to "1". When the flip-flop is in the "1" state, the "1" output shown on the "1" side of the symbol is positive, and when in the "0" state the output on the "0" side is positive.

It is sometimes desirable to simply reverse the state of a flip-flop by an input signal. This is done by applying a "trigger" signal simultaneously to both input lines through isolation crystals outside the flip-flop circuit. The sample circuit shown in Figure 12 includes a trigger input line, connected to CR05 and CR06. A negative COMPLEMENT X pulse on this line is received, through the crystals, by both sides of the flip-flop. The signal has no direct effect on the non-conducting triode, but proceeds to cut off the conducting triode. As a result, the state of the flip-flop is reversed in the manner described above.

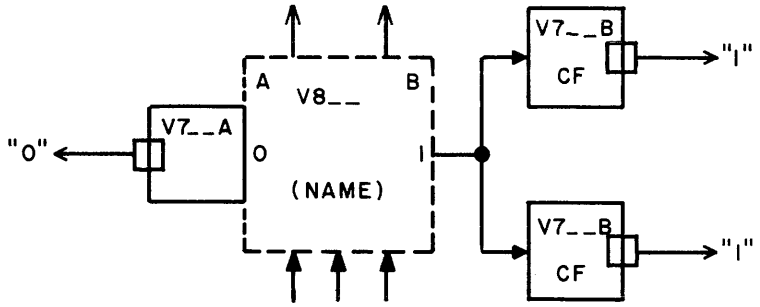
(2) CATHODE FOLLOWER. - The standard cathode follower stage is essentially an impedance matching device. In Figure 4, the low impedance cathode output voltage "follows" closely the changes in potential of the high impedance input, hence the name cathode follower. A triode vacuum tube (1/2-5963) is employed with its plate tied to +150vdc. The cathode is connected through a resistance to -80vdc. The output of the cathode follower is taken across the cathode resistor.

In actual operation, a positive signal from the output of a flip-flop is fed directly into the grid of the cathode follower tube. This causes the cathode to draw current and results in a voltage drop across the cathode resistor. Since the output voltage is taken across the cathode resistor, this voltage drop causes the output to change relative to the input signal. When the flip-flop changes state and the input signal is removed, the cathode ceases to draw current and the output signal is correspondingly removed. The particular side, A or B, of the 5963 tube used is included in the tube's symbol series number.

(3) INVERTER. - The standard inverter circuit is essentially a phase inverter which is used to reverse the polarity of the input signal. A signal triode (1/2-5963) is used and it is shown with its associated circuitry in Figure 5.



CATHODE FOLLOWER CIRCUIT



SHORTHAND SCHEMATIC SYMBOL *

SYMBOL SERIES NUMBERS V70 THROUGH V79 AND V90 THROUGH V99 FOLLOWED BY "A" OR "B" ARE ASSIGNED TO THE CATHODE FOLLOWER AND INVERTER TUBES.

* WHEN MORE THAN ONE CATHODE FOLLOWER IS USED ON A SINGLE FLIP-FLOP OUTPUT, THE CATHODE FOLLOWER SYMBOLS ARE SHOWN DETACHED FROM THE FLIP-FLOP BLOCK ON SCHEMATIC-TYPE DIAGRAMS

Figure 4. STANDARD Cathode Follower Stage
PX 131

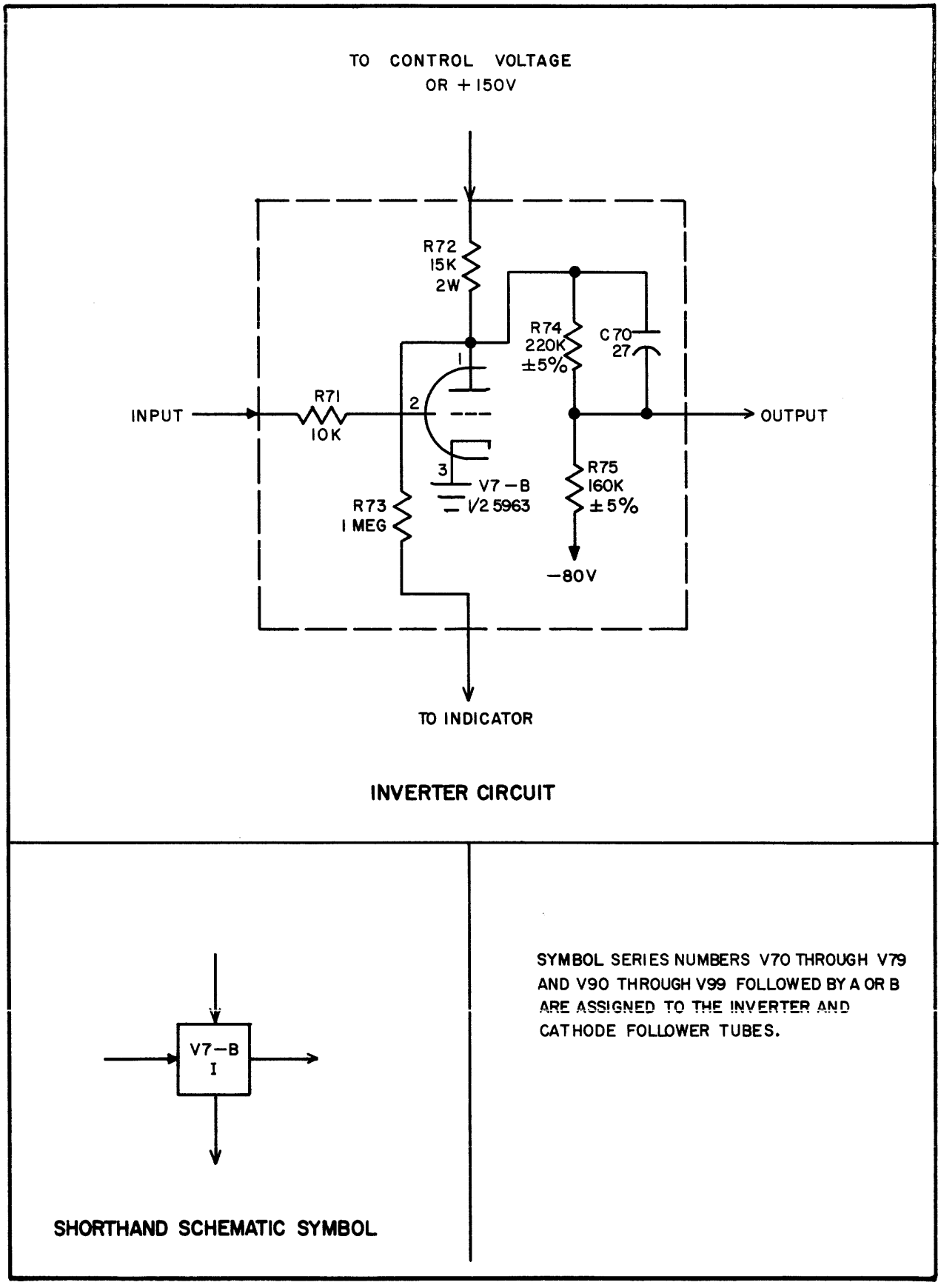


Figure 5. STANDARD Inverter Stage
PX 131

In actual operation, a positive signal arrives at the input and is fed into the grid of the inverter. This increase in grid voltage causes the plate circuit to draw current with a resulting decrease in plate voltage. The decrease in plate voltage is distributed in the voltage divider R74, R75 and causes the output to be driven to a negative state.

When the positive signal is removed from the input, the grid voltage is reduced. This reduction causes the plate current to decrease and the plate voltage to increase. The resultant increase in plate voltage is distributed in the voltage divider R74, R75 and causes the output to return to its positive state. Thus, when a positive signal is applied to the input, a negative signal results in the output. Conversely, when no signal is applied to the input, a positive signal results in the output. The particular side, A or B, of the 5963 tube is included in the inverter's symbol series number.

(4) GATE. - The standard gate circuit regulates the passage of signal pulses. It may either pass or block a signal pulse depending upon the presence of a positive d-c potential called the "enable" at the suppressor grid. A pentode (7AK7) is used in the circuit shown in Figure 6. The plate is connected to +150vdc through a load. The screen grid is tied to +100vdc.

In actual operation, a pulse arrives at the input and is fed into the control grid. If a positive d-c potential (enable) is coincidently fed into the suppressor grid via the external enable circuit, the plate then draws current and a resultant pulse signal is formed in the output circuit. Thus the tube has effectively passed the pulse signal. If the pulse signal arrives at the input and a d-c enable is not fed into the suppressor grid, the plate does not draw current and no resultant signal is produced in the output circuit. Thus the tube has effectively blocked the pulse signal.

(5) AMPLIFIER. - The standard amplifier is used to produce voltage gain. A 6AN5 tube is used and is shown in its typical circuit in Figure 7.

In operation, a pulse signal arrives at the input and is fed into the control grid. The pulse causes the control grid to be driven to a relative positive state which causes the plate circuit to draw current. A voltage drop is formed across the plate load, which is much larger than the original input signal. In this manner, voltage gain has been produced, and the original input signal has been amplified.

(6) PULSE TRANSFORMERS. - Standard pulse transformers are used primarily for impedance matching and phase inversion purposes.

In actual operation, the pulse transformer does not differ greatly from an ordinary transformer. However, care was taken in construction to provide the pulse transformer with sufficient high and low frequency response to avoid distorting the pulse wave shape as it passes.

Winding ratios, as well as other symbols, are shown on each diagram as indicated in Figure 8.

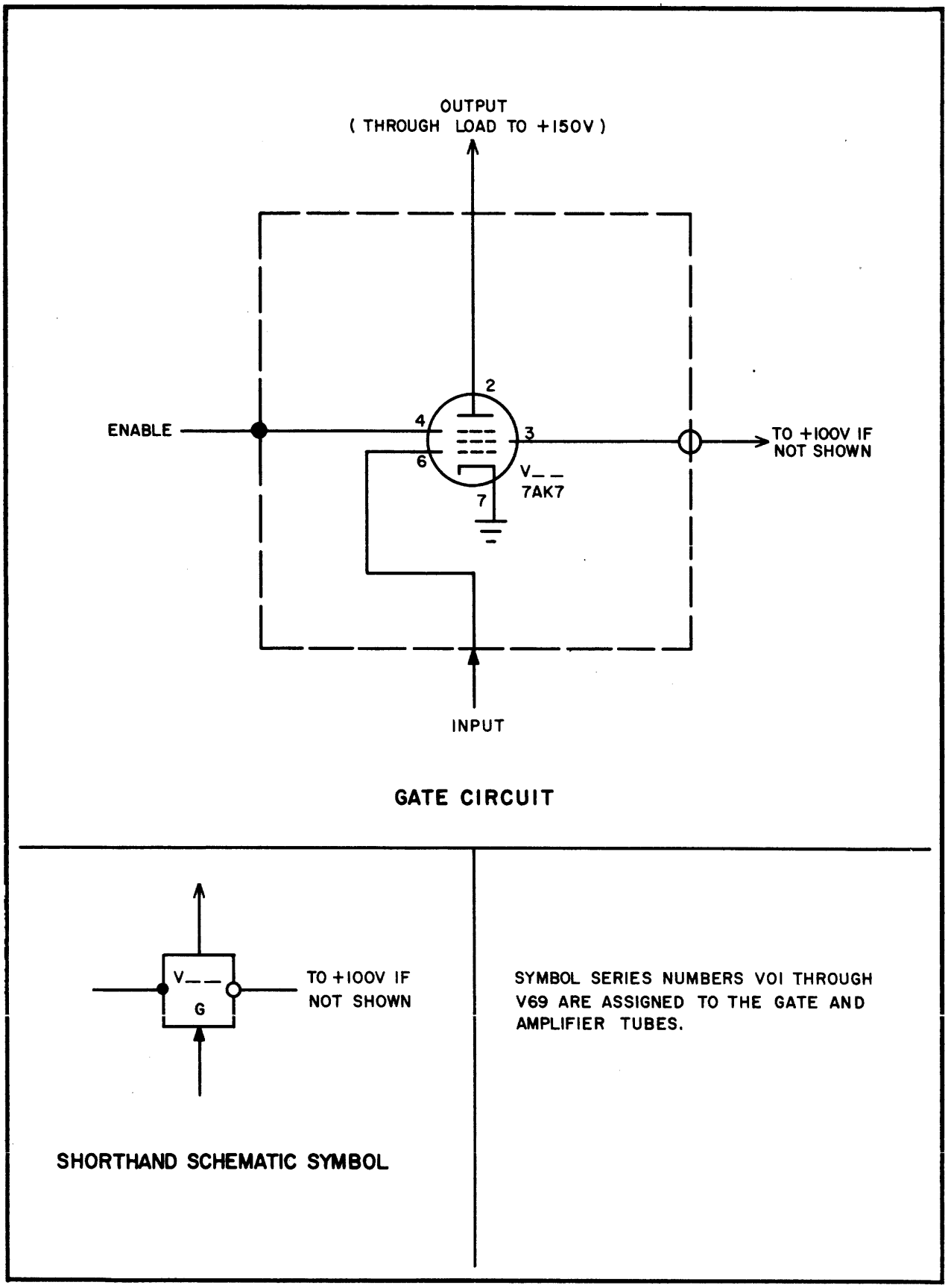
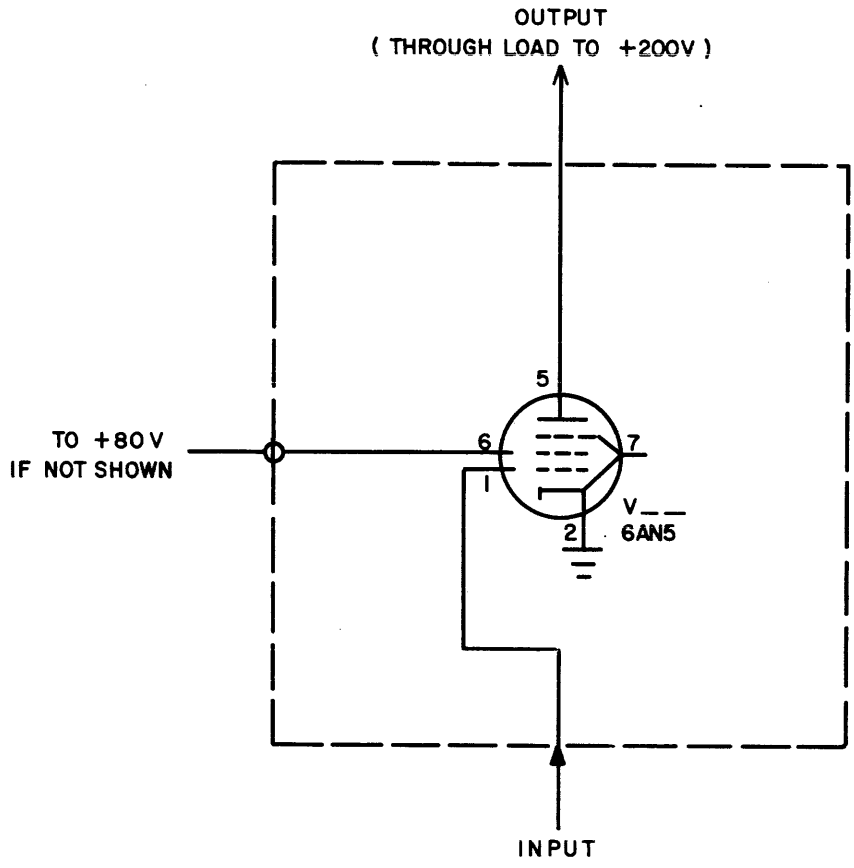
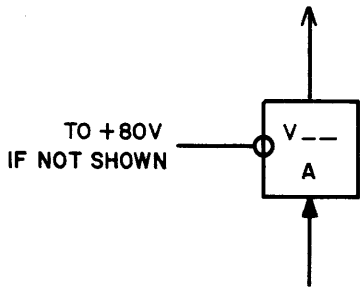


Figure 6. STANDARD Gate Stage
PX 131



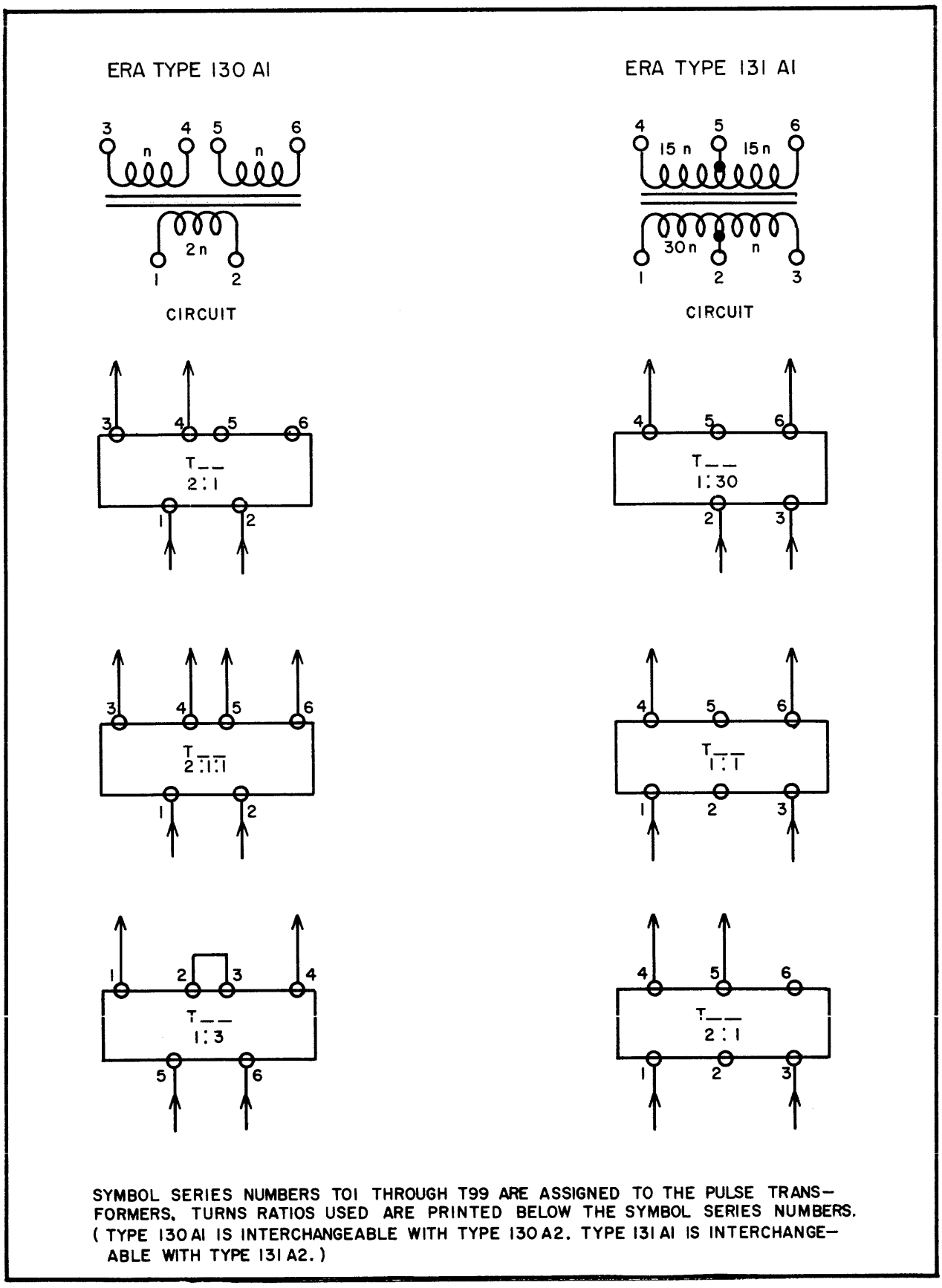
AMPLIFIER CIRCUIT



SHORTHAND SCHEMATIC SYMBOL

SYMBOL SERIES NUMBERS V0I THROUGH V69 ARE ASSIGNED TO THE AMPLIFIER AND GATE TUBES.

Figure 7. STANDARD Amplifier Stage
PX 131



SYMBOL SERIES NUMBERS T01 THROUGH T99 ARE ASSIGNED TO THE PULSE TRANSFORMERS. TURNS RATIOS USED ARE PRINTED BELOW THE SYMBOL SERIES NUMBERS. (TYPE 130 A1 IS INTERCHANGEABLE WITH TYPE 130 A2. TYPE 131 A1 IS INTERCHANGEABLE WITH TYPE 131 A2.)

Figure 8. STANDARD Pulse Transformer Stages
PX 131

(7) SHAPER. - A shaper is used to change the form of a pulse to a desired level, duration, or shape. This is done in order to facilitate the use of the pulse in a special application or circuit. Shapers differ in their purpose and circuitry. For this reason, shapers are indicated by the symbol shown in Figure 9, and their operations are not detailed unless necessary for the explanation of an associated circuit.

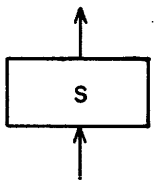


Figure 9. Shaper Symbol

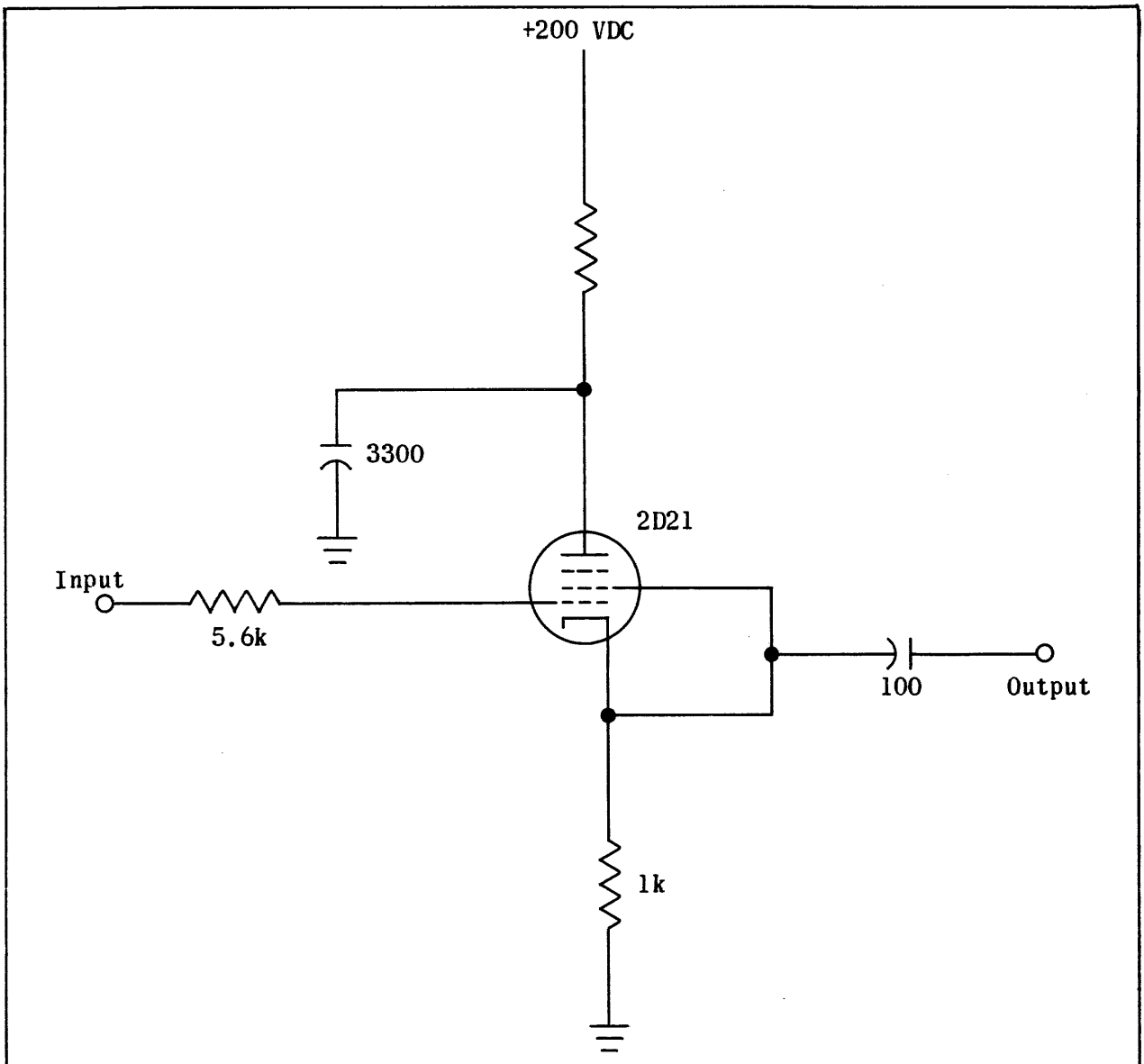
(8) SINGLE PULSE CIRCUIT. - A standard single pulse circuit is used to provide a single pulse output when its input has been triggered by a positive d-c potential. It generally consists of a thyratron type 2D21 tube and its associated circuitry as shown in Figure 10.

In actual operation, the input signal is fed into the control grid. The characteristics of a thyratron are such that, if the input signal potential is great enough, the tube suddenly discharges and forms a short but strong output pulse in the cathode circuit. An output signal is also produced in the plate circuit, but it is not used in this application. After the discharge, the thyratron returns to its original state and is ready for the next input signal.

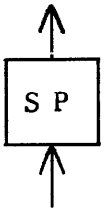
(9) DELAY (VACUUM TUBE). - The standard vacuum tube delay network causes a short delay to the passage of an input pulse. A 5963 tube is used and is shown with its associated circuitry in Figure 11.

In actual operation, the B section of the tube is normally conducting, while the A section is normally cut-off. When a negative going pulse is fed into the input, the grid of the B section is driven negatively and causes it to be cut off. The plate voltage increase, resulting from the cut off of section B, is fed into the grid of section A, which causes it to conduct. The result is a reduction in the plate voltage of section A. Simultaneously with the above operations, the capacitor (C09) was discharged by the input pulse. It begins immediately to recharge and, upon its recovery, causes the tube to switch back to its original state. This causes an increase in the plate voltage of section A.

The momentary reduction and resultant restoration of the plate voltage of section A is fed through the capacitor (C11), which translates the reduction and restoration into a single negative and single positive pulse. The actual delay in time is represented by the interval between these two pulses. When these pulses are fed into the cathode follower circuit, the negative pulse is ignored and the positive pulse is passed. The resultant pulse, which appears at the output, is delayed, as compared to the original input pulse.



Single Pulse Circuit



Shorthand Schematic Symbol

Figure 10. STANDARD Single Pulse Circuit
PX 131

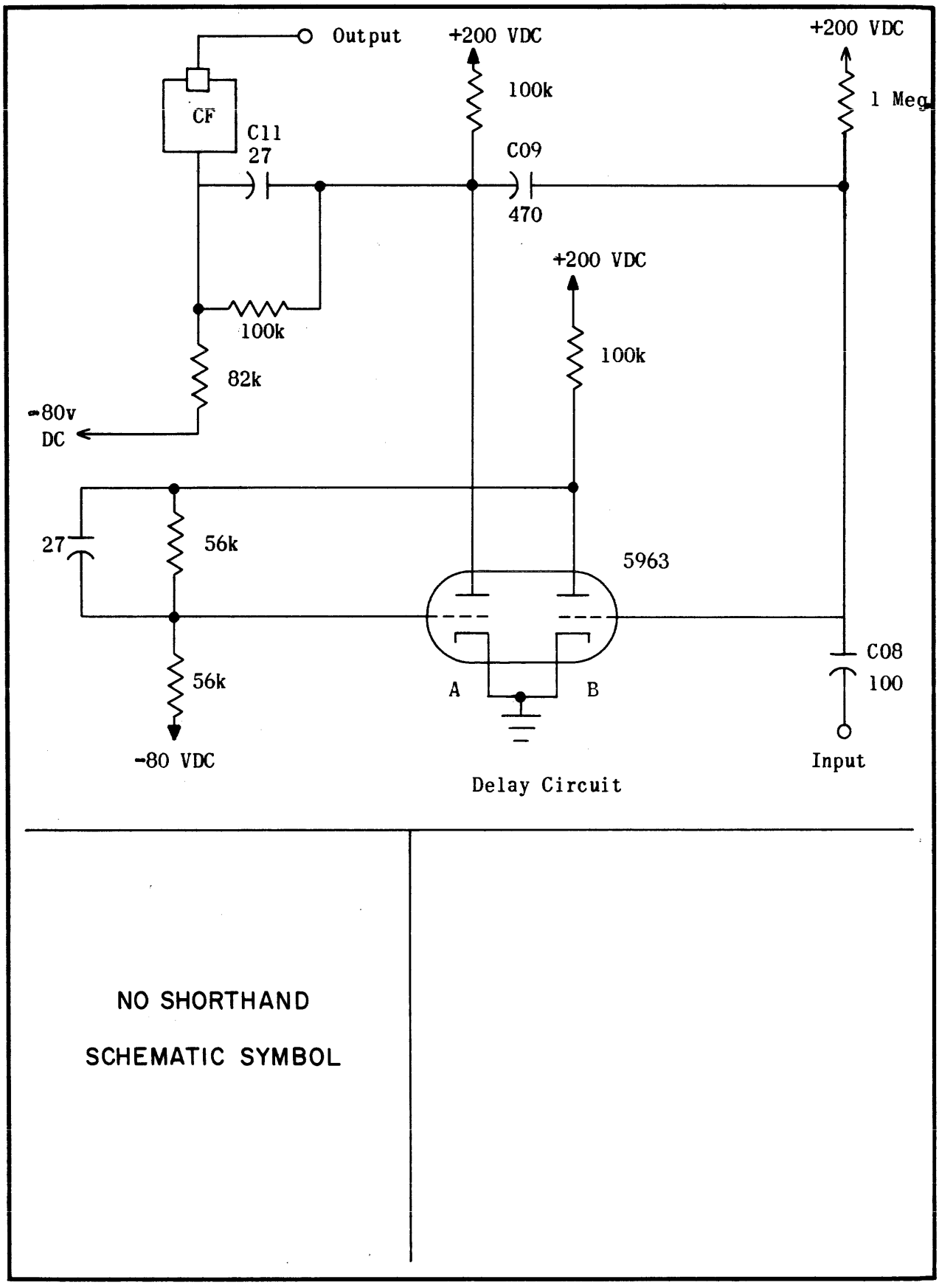


Figure 11. STANDARD Delay Circuit (Vacuum Tube)
PX 131

(10) SUMMARY. - To illustrate how some of these shorthand schematic symbols are used, a portion of a typical schematic-type diagram is shown in Figure 12.

4. UNIT CHASSIS CONSTRUCTION.

The pluggable unit chassis used in the computer are constructed on a standard basis. A typical unit chassis is shown in Figure 13. Tubes, pulse transformers, and relays are mounted on the tube channels on top of the chassis; circuit components, such as resistors, crystals, pulse transformers, and capacitors, are mounted on two terminal boards mounted within the chassis; and capacitors and pulse transformers are sometimes mounted below the terminal boards on the chassis frame. Mounted on the chassis base is a male plug, which fits into a female jack in one of the computer cabinets. Unit chassis are constructed by using the unit symbol series system and the coordinate system to identify and locate the circuit components on the chassis. These two systems are explained below.

a. SYMBOL SERIES SYSTEM. - The unit chassis in the 10000, 30000, and 60000 cabinets are constructed with this system. The name of a component, such as R70 or CR80, is lettered on the terminal board between the connection lugs. A typical terminal board for the symbol series system is shown in Figure 14.

If, in trouble shooting a chassis, a certain crystal is suspected as the cause of the trouble, the crystal can be located on the unit signal diagram, and then, by using the crystal name, it can be located on the unit chassis itself and tested.

When the trouble is in a circuit which is part of one of the standard symbols, such as a flip-flop, the tube number is taken from the unit signal diagram, and the tube is located on the tube channel on top of the chassis. The component array that is associated with this tube is located by the lettered letters on the terminal boards. For example, a flip-flop V80 is found on the tube channel, and its component array located by looking on the terminal board for FF80.

b. COORDINATE SYSTEM. - The unit chassis in the 55000 cabinet and the Magnetic Tape Storage System (70000 cabinet) are constructed with this system. In the coordinate system the component names are not lettered on the terminal boards, but rather the name of the component on the unit signal diagram includes its coordinate location on the terminal boards. Figure 15 shows a typical coordinate terminal board. As the board is viewed with the unit chassis number at the top, there are 10 lug positions vertically labelled 0 through 9, and 30 lug positions horizontally labelled 01 through 29.

To further facilitate the location of components, the sides of the terminal boards are designated A and B for one board, and C and D for the other board. The A side and the D side of the two terminal boards are always on the outside of the chassis. The components which are susceptible to failure are then mounted on the A and D sides for ease of accessibility. A typical schematic type diagram using the coordinate system of identification is shown in Figure 16.

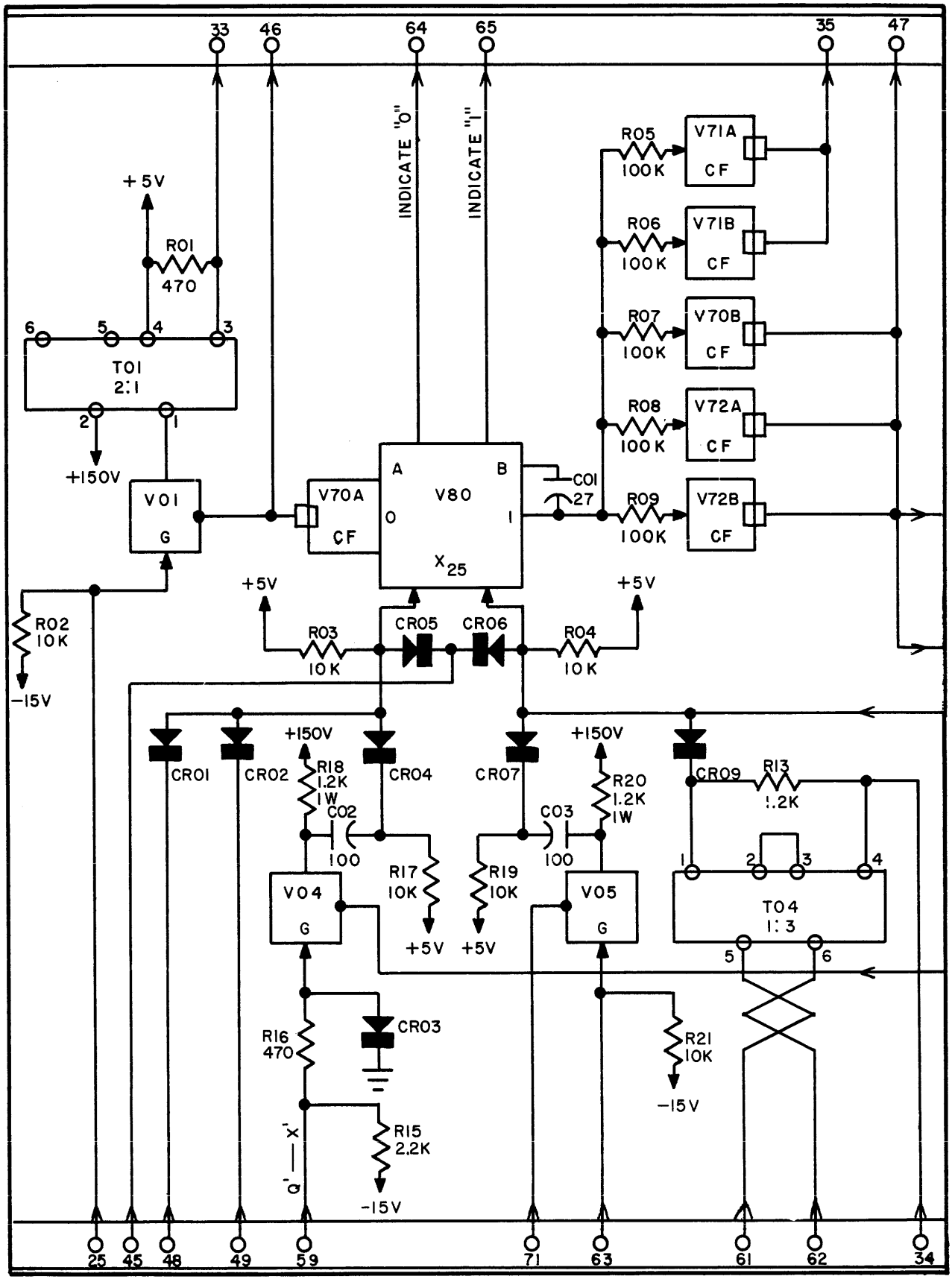


Figure 12. Portion of a Typical Schematic Diagram
(Symbol Series System)
PX 131

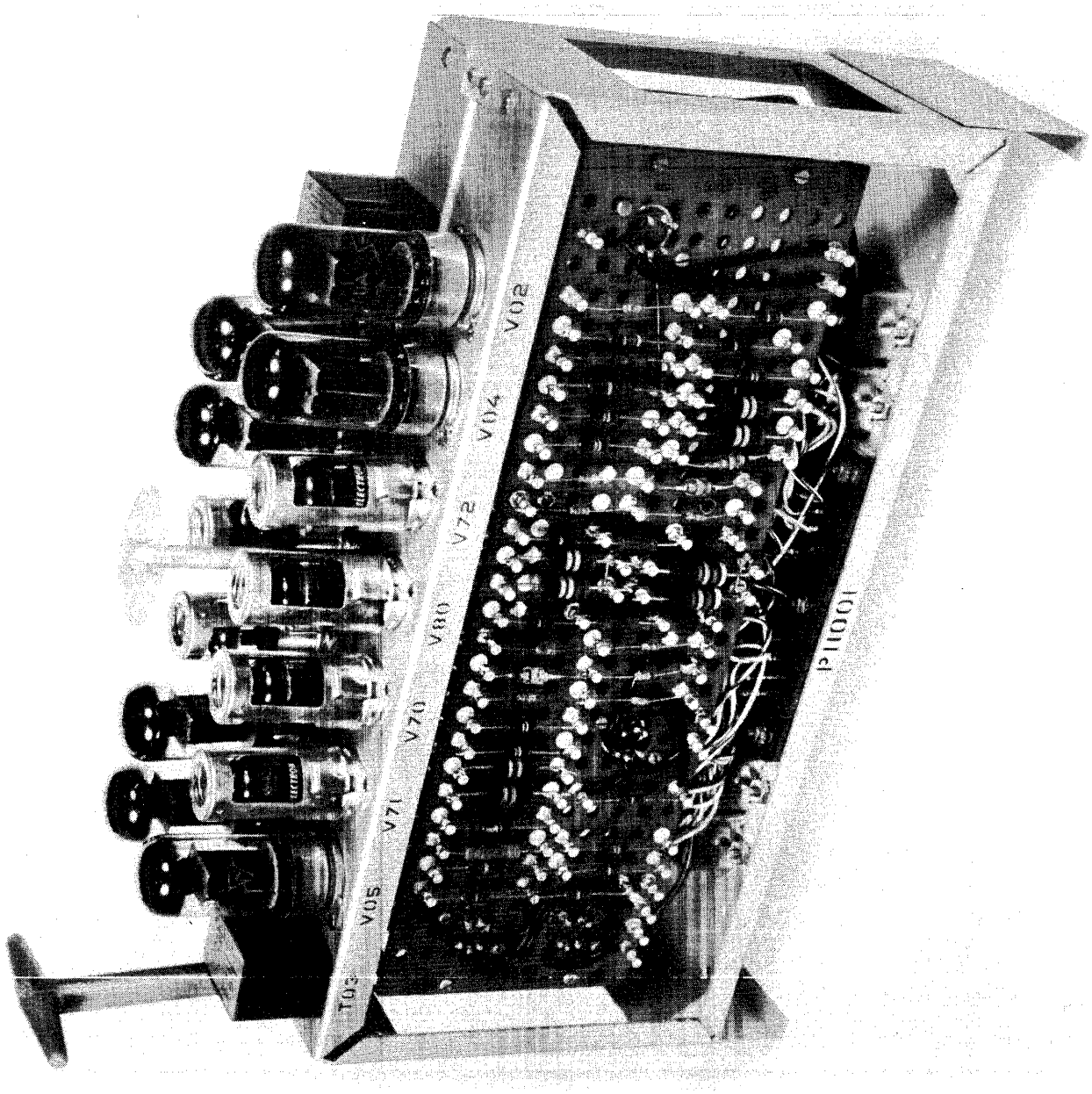


Figure 13. Typical Unit Chassis
PX 131

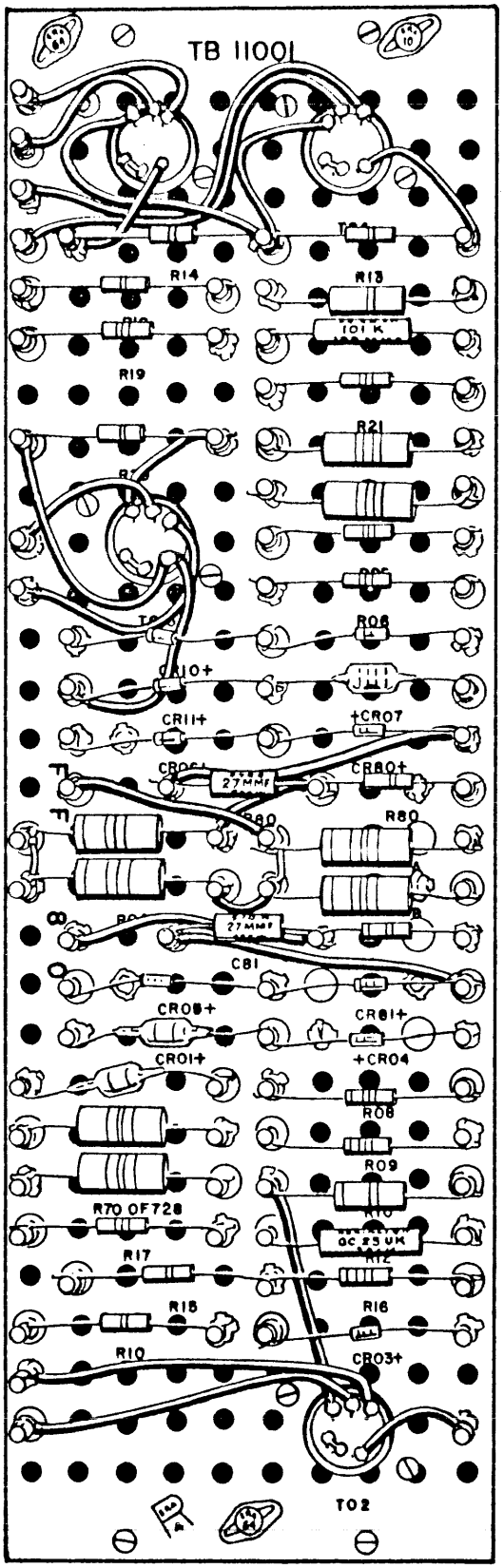


Figure 14. **Terminal Board (Symbol Series System)**
PX 131

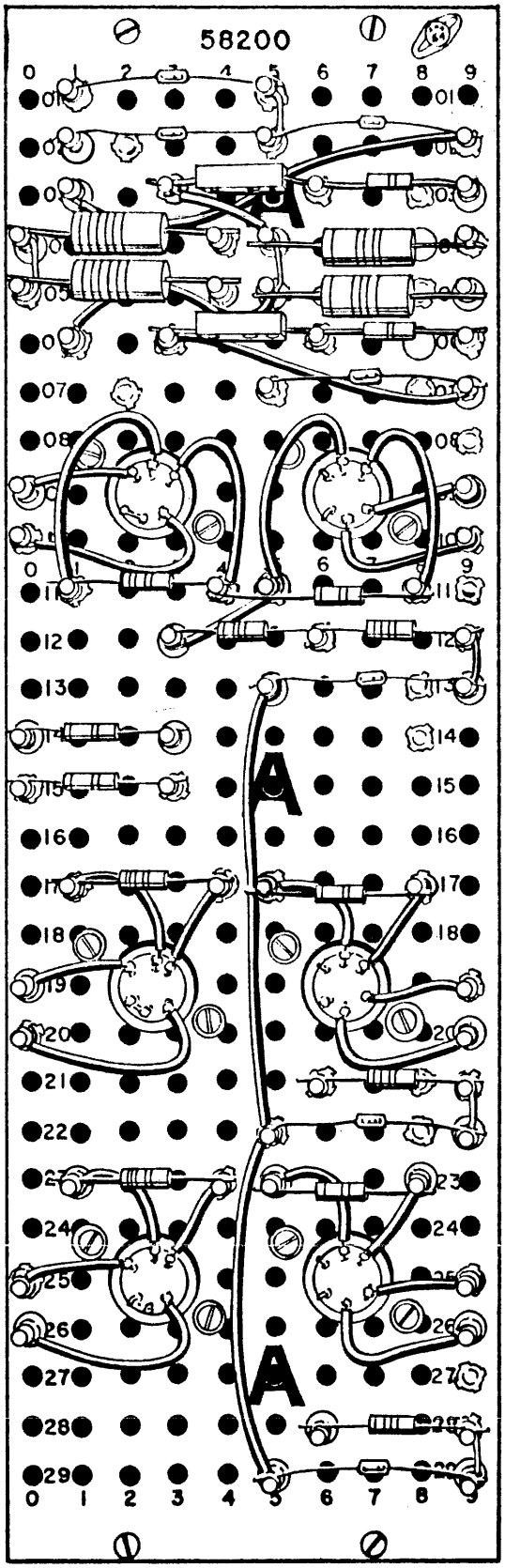


Figure 15. **Terminal Board (Coordinate System)**
PX 131

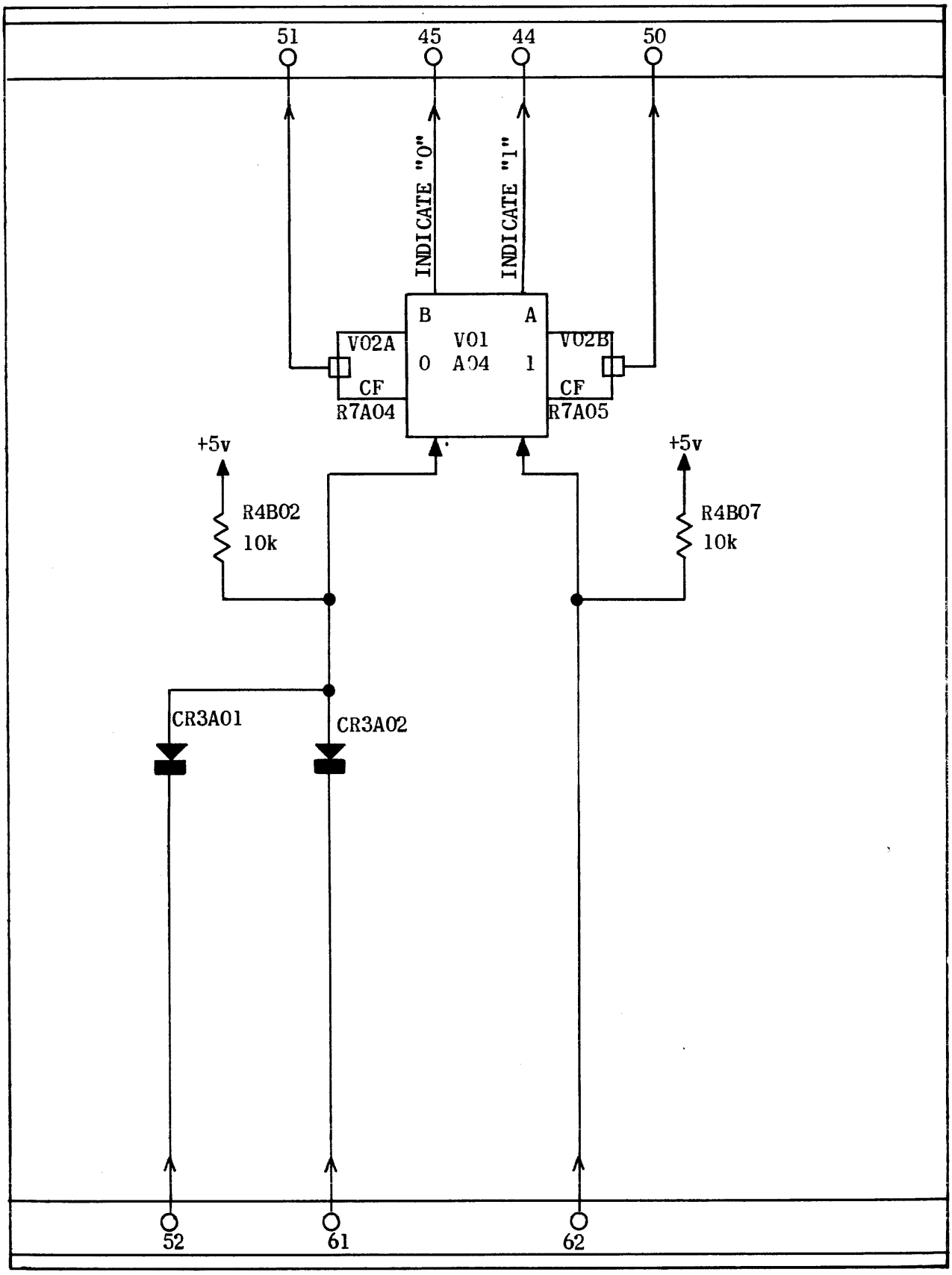


Figure 16. Portion of a Typical Schematic Diagram (Coordinate System)
PX 131

A particular component, such as a CR3A01, in Figure 16, is located on the terminal board (Figure 15) in the following manner. The CR indicates that it is a crystal, the 3 is the vertical ordinate, the A indicates that the component is on the A side of the A/B terminal board, and the 01 is the horizontal ordinate. To find the component on the chassis, you find the point at which the 3 vertical ordinate and the 01 horizontal ordinate cross on the A side of the A/B terminal board. The crystal is mounted above this point. The other individual components are located in the same manner.

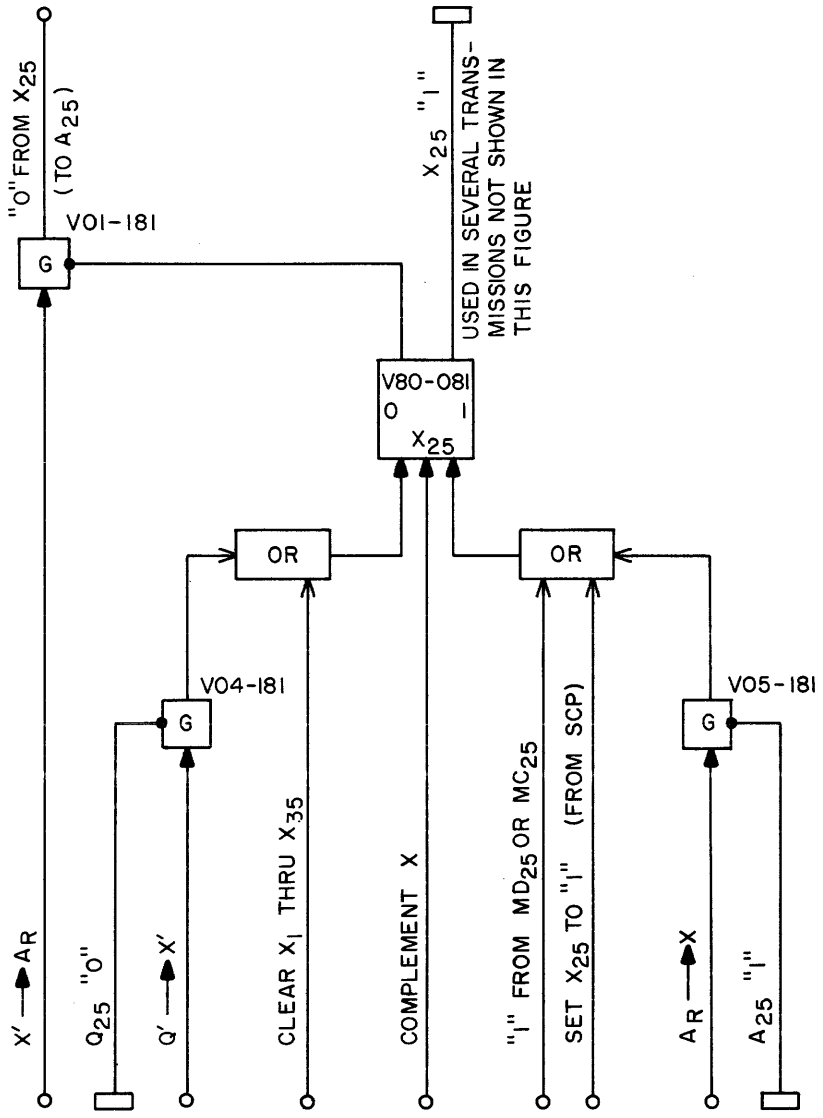
The location of a flip-flop involves the location of the tubes on the tube channel and the component array on the terminal board. There are two numbers in the shorthand symbol for a flip-flop, designating the tube location on the tube channel and the component array on the terminal board. The tube V01 for the flip-flop shown in Figure 16 is found at tube channel location V01, and the component array for the flip-flop is at location A04. This means the 04 horizontal ordinate on the A side of the A/B terminal board bisects the component array of this flip-flop. There are additional components for this flip-flop on the B side of this terminal board immediately below the components on the A side.

5. BLOCK DIAGRAMS AND UNIT SIGNAL DIAGRAMS

Figure 12 is a portion of a schematic diagram for a stage of the X Register. Figure 17 is the same circuitry shown in the block diagram form using block diagram symbols. All circuit components on the schematic diagram are not shown on the block diagram. This is because only those components which have a "logical" function, that is, which actually effect the logic of the computer system, are shown on the block diagram.

In the block diagrams each component which consists of a tube is noted by the tube number and three digits, such as V80-081. On the block diagram is a note which provides the series of jack numbers on which the tubes are located. In this case Figure 17 indicates that these components are found on unit signal diagrams in the 10000 series. Therefore, V80-081 is tube number V80 on the unit signal diagram for the 10081 jack location. The other components are located in the same manner.

In some cases on the block diagrams a "1" enable from a flip-flop is shown applied to a gate, and, when the unit signal is checked, it is found that the enable is actually taken from the "0" side of the flip-flop and inverted before it is applied to the gate. This is done for component efficiency when the "1" side of the flip-flop is supplying many enables. These are shown on the block diagrams as "1" enables, because, logically, the "0" enable inverted is seen electrically as a "1" enable.



NOTE: THE NUMBERS SUCH AS V80-081 DENOTE TUBE NUMBERS AND 10000 SERIES JACK NUMBERS i.e. V80, J10081, UNLESS THE JACK IS OTHERWISE NOTED

Figure 17. Block Diagram Representation
PX 131

SUPERVISORY CONTROL PANEL

1. GENERAL

The Supervisory Control Panel is located in the 40000 cabinet. This panel provides manual controls for loading and operating the computer in several modes, and indicators for a visual indication of the step-by-step sequences involved. An overall view of the Supervisory Control Panel is shown in Figure 1.

The groups of pushbuttons and switches located on the center switch panel are used to select the NORMAL mode of operation, any one of several TEST modes, a manual interrupt, and programmed jumps and stops. On the left switch panel are two groups of controls used in the testing of the Magnetic Tape Storage System, an OPERATING TIME meter which provides an indication, in seconds, of the duration the equipment is in operation, an ON-OFF control for the Photoelectric Tape Reader, and an ON-OFF control and TAPE FEED control for the High-Speed Punch.

The indicator panels contain translator indicators, flip-flop indicators, and flip-flop set and clear buttons. Most of these buttons and indicators are normally used during the low-speed TEST modes of operation. The left indicator panel contains Magnetic Tape Storage System buttons and indicators, the IOB input-output system buttons and indicators, the IOA input-output system buttons and indicators, and the control flip-flop indicators for the IOA-IOB systems. The right indicator panel contains Magnetic Core Storage System, Magnetic Drum Storage system, Typewriter, and High-Speed Punch buttons and indicators. Between these two panels is the center indicator panel, which contains buttons and indicators for the Control and Arithmetic sections of the computer. An Address Monitor scope is located at the top of the panel.

Where a pair of lamps is used to indicate a flip-flop, the glowing of the upper lamp indicates a "1", and the lower lamp indicates a "0". The blue and black buttons are "set" buttons, used to set individual flip-flops to "1"; and the white buttons are "clear" buttons, used to clear one or more flip-flops to "0".

2. LOWER PANEL

The left switch panel, the center switch panel, and the right switch panel controls are shown in detail in Figures 2, 3, and 4 respectively. These pushbuttons and indicators are grouped by their function. By using these controls, the maintenance personnel can initiate computer operation at several pulse repetition rates and set up various test conditions. In this volume the groups are given descriptive names and are discussed below in the order in which they are arranged from left to right on the panel. They are named as follows:

1) Left Switch Panel

   a) Operating Time Meter
   b) Tape Punch Group

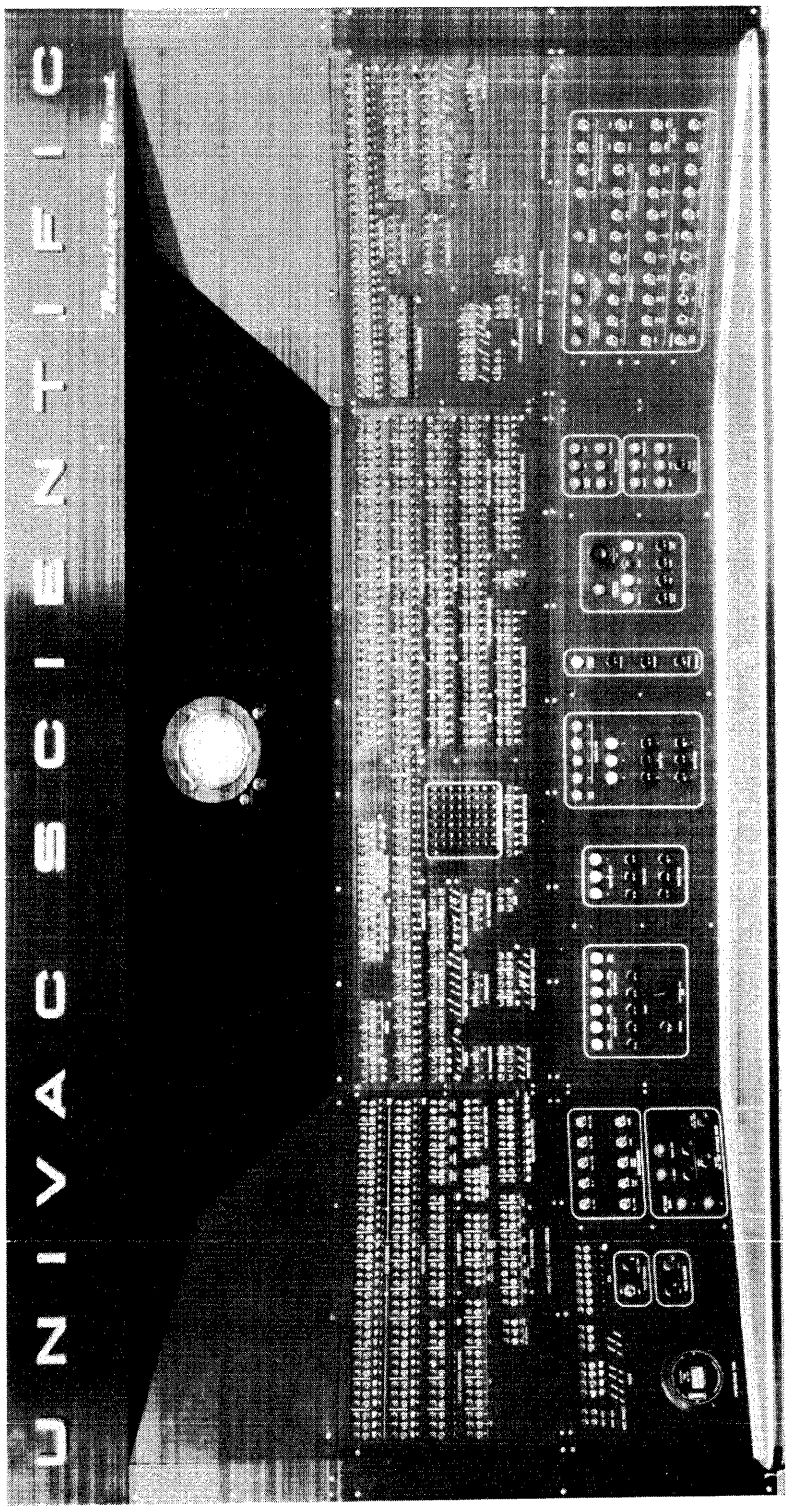


Figure 1. Supervisory Control Panel, Overall View
PX 132

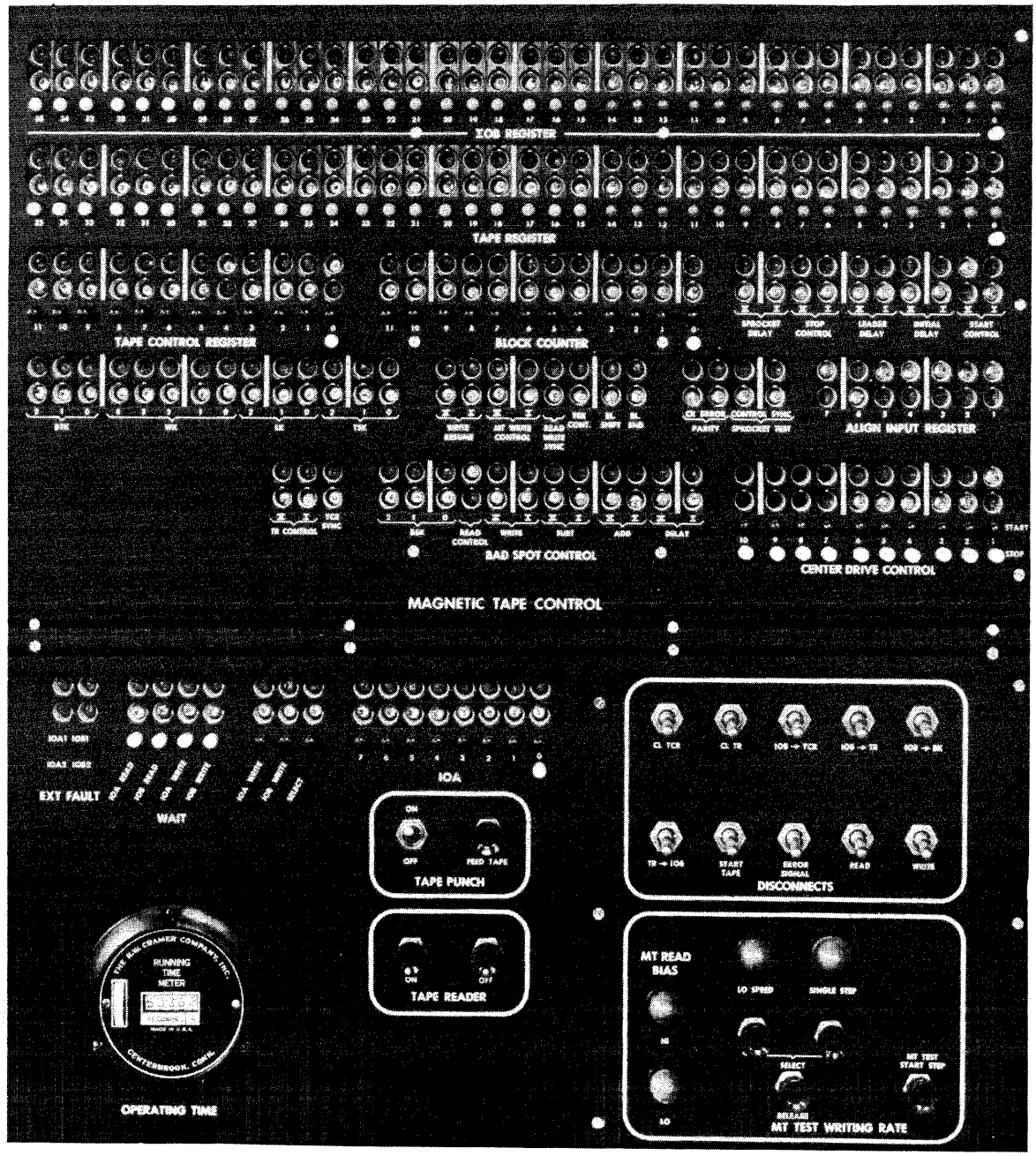


Figure 2. Supervisory Control Panel, Left Section

PX 132

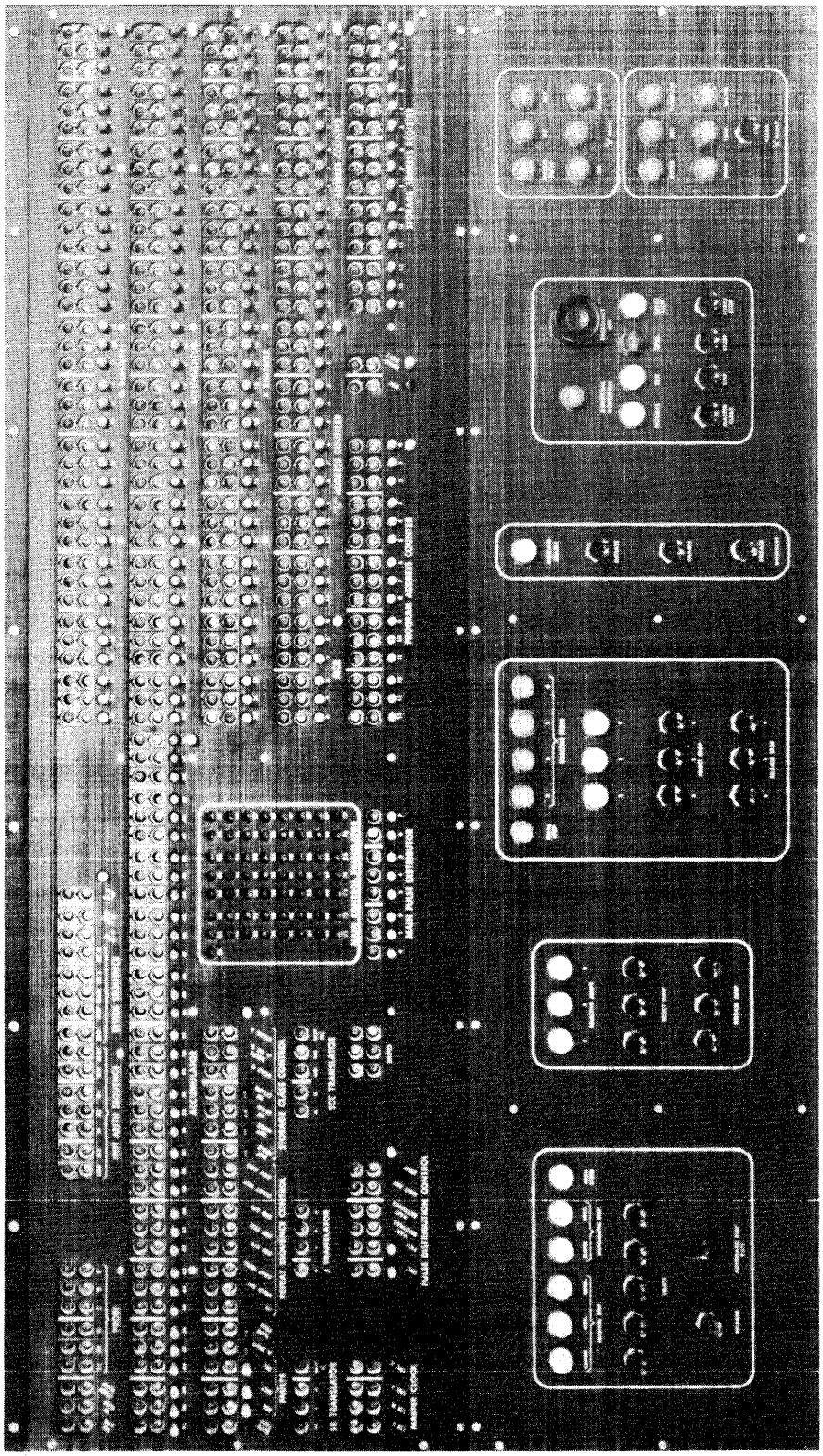


Figure 3. Supervisory Control Panel, Center Section
PX 132

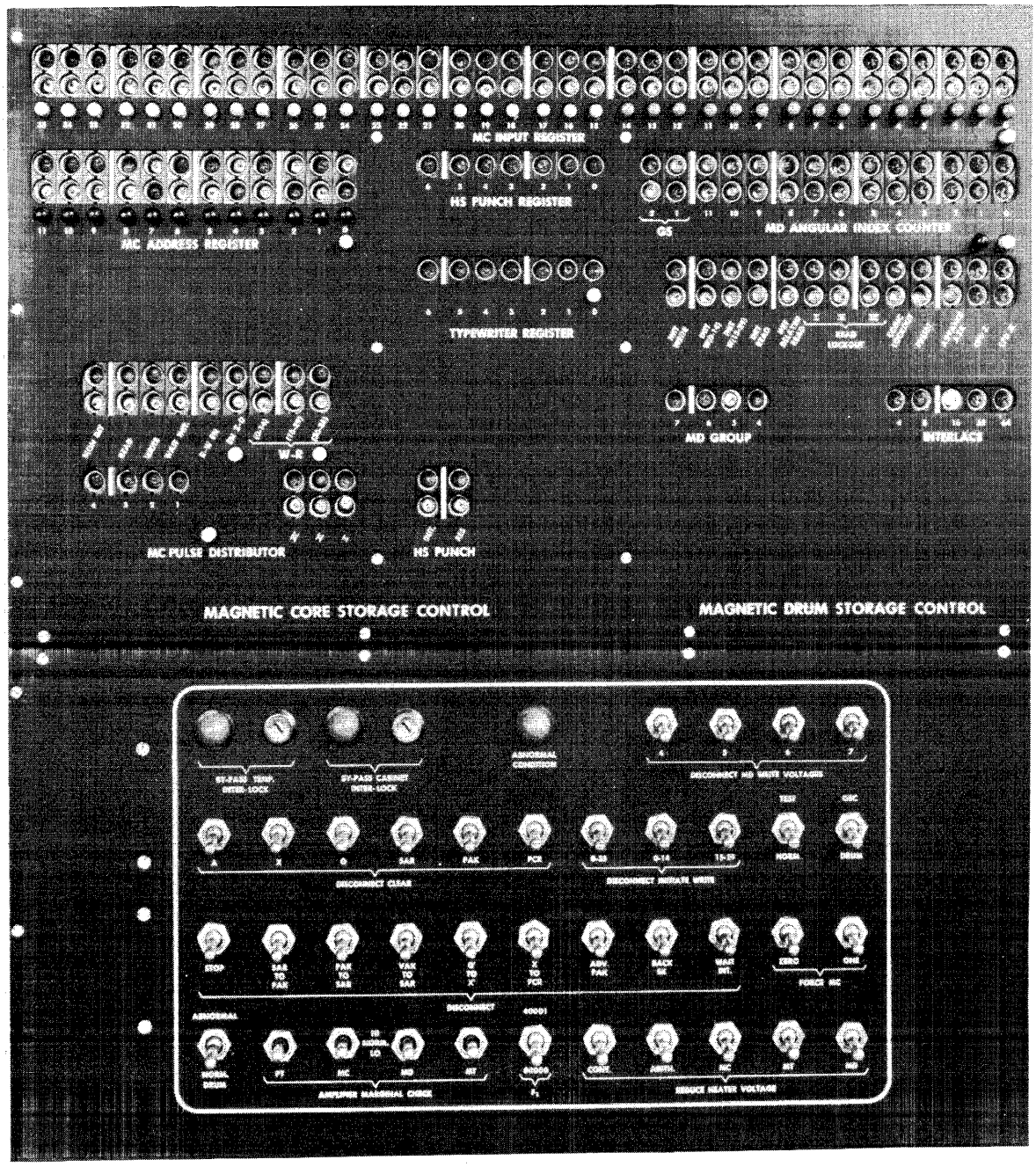


Figure 4. Supervisory Control Panel, Right Section
PX 132

c) Tape Reader Group
d) MT Disconnects Group
e) MT Test Writing Rate Group

2) Center Switch Panel

a) Operating Rate Group
b) Selective Jumps Group
c) Selective Stops Group
d) Program Interrupt Group
e) Operating Group
f) B Fault Group
g) A Fault Group

3) Right Switch Panel

a) Test Switch Group

If no test selections have been made, the computer is ready to operate in the NORMAL mode at HIGH SPEED. The TEST mode of operation is automatically selected if a selection is made in the Operating Rate Group, if the MD NORMAL-ABNORMAL switch in the Test Switch Group is placed in the up position, or if the TEST-NORMAL switch in the Test Switch Group is placed in the up position. Removing all of these selections returns the computer to the NORMAL mode and selects HIGH SPEED as the operating rate.

a. OPERATING TIME METER. - The Operating Time Meter visually registers the operating time of the equipment in seconds and tenths of seconds and is controlled by the start and stop circuitry of the equipment. The meter is equipped with a thumb wheel which permits manual resetting to zero.

b. TAPE PUNCH GROUP. - The controls in this group are used by the operator to turn the High-Speed Punch on and off and to feed the paper tape manually.

c. TAPE READER GROUP. - The ON-OFF control in this group is used to turn on and off the Photoelectric Tape Reader motor.

d. MT DISCONNECT GROUP. - The switches in this group are used by maintenance personnel during test procedures to disconnect certain circuits within the Magnetic Tape System. These selections can be made only when the TEST mode has been selected. When any of these switches are placed in the "up" position, the +80vdc on the screen grid of an amplifier in the appropriate circuit is removed so that the signal is disconnected. For example, placing the TR $\longrightarrow$ 10B switch in the "up" position disconnects the +80vdc on the screen grids of amplifiers V23 and V24 in jack 70253. With the +80vdc removed, a -80vdc is applied to the screen grid through a divider network so that the grid becomes negative and the TR $\longrightarrow$ 10B signal does not pass.

e. MT TEST WRITING RATE GROUP. - The MT Test Writing Rate Group push-buttons and relays provide a means for manually selecting Lo Speed or Single Step, and for starting or stopping the computer writing operations in the TEST mode. No selection can be made in the MT Test Writing Rate Group until TEST has been previously selected. A thorough analysis of this group is given in the volume on the Magnetic Tape System.

f. OPERATING RATE GROUP. - This group consists of five step operation selectors with their associated indicators, a HIGH-SPEED indicator, an AUTOMATIC STEP RATE potentiometer, and a group RELEASE button. If none of the step operations have been selected in this group, HIGH SPEED is automatically selected as the clock rate. The HIGH SPEED selection causes the system to function continuously at a 500kc clock pulse rate, supplied by either the Magnetic Drum or the Test Oscillator, depending on the position of the DRUM-OSCILLATOR switch in the Test Switch Group. If the equipment is set up to operate in the NORMAL mode at HIGH SPEED, and a step operation selection is made, the equipment switches to the TEST mode of operation and the HIGH SPEED selection is dropped. Pressing the RELEASE button drops the selected rate and automatically returns the equipment to the NORMAL mode and HIGH SPEED. To select HIGH SPEED in the TEST mode, it is necessary to select TEST by placing the TEST-NORMAL switch in the Test Switch Group in the TEST position.

The MANUAL STEP CLOCK selection causes one clock pulse to be produced each time the STEP button in the OPERATING group is pressed. The MANUAL STEP DIST. selection causes the Main Pulse Distributor to be advanced one position, or one reference operation to be performed each time the STEP button is pressed. The MANUAL STEP OPERATION selection causes one complete instruction to be executed each time the STEP button is pressed. The AUTOMATIC STEP CLOCK selection allows the system to function at a clock pulse rate determined by the AUTOMATIC STEP RATE potentiometer adjustment. Pressing the AUTOMATIC STEP OPERATION selector causes the system to function at an instruction execution rate determined by the AUTOMATIC STEP RATE adjustment. The AUTOMATIC STEP RATE control is a potentiometer which provides a 5-35cps adjustment for the two AUTOMATIC STEP selections described above.

g. SELECTIVE JUMPS GROUP. - Three SELECT JUMP selectors, their associated indicators, and three RELEASE JUMP selectors are located within this group. The SELECT JUMP 3, 2, and 1 selectors provide for optional execution of programmed Manually Selective Jump 1, 2, and 3 instructions. The RELEASE JUMP selectors 3, 2 and 1 permit release of the previous jump selections when the equipment is not in operation.

h. SELECTIVE STOPS GROUP. - This group consists of five stops indicators, three SELECT STOP buttons and their associated indicators, and three RELEASE STOP selectors. The SELECT STOP 3, 2, and 1 selectors provide for optional execution of programmed Manually Selective Stop 3, 2, and 1 instructions. The FINAL STOP indicator is illuminated when computation has been completed as dictated by a programmed Final Stop instruction. SELECTIVE STOP indicator 3, 2, or 1 is illuminated when a previously selected Manually Selective Stop 3, 2, or 1 instruction is executed. The 0 STOP indicator illuminates when a programmed Manually Selective Stop 0 is executed. Pressing a RELEASE STOP button at any time during system operation drops the corresponding STOP selection.

If a FINAL STOP indication occurs, it is necessary to master clear before restarting.

i. PROGRAM INTERRUPT GROUP. - An INDICATE ENABLE indicator, an ENABLE button, an INITIATE button, and a RELEASE button comprise this group. These controls provide a means of manually interrupting the program in progress. To prevent an unintentional interrupt it is necessary to energize the manual

interrupt circuitry by pressing the ENABLE button. This causes the INDICATE ENABLE indicator to illuminate. Pressing the INITIATE button accomplishes the interrupt and extinguishes the INDICATE ENABLE indicator. The RELEASE button can be used to drop the enable if the operator does not manually interrupt.

j. OPERATING GROUP. - This group consists of the NORMAL, TEST, OPERATING, FORCE STOP, and ABNORMAL CONDITION indicators and the MASTER CLEAR, STEP, START, FORCE STOP, AND EMERGENCY OFF selectors. If the TEST mode has not been selected, the NORMAL indicator glows. This indicates that, when the START button is pressed, the computer will operate at HIGH SPEED in the NORMAL mode of operation. If the TEST mode has been selected, the TEST indicator is illuminated. When the START button is pressed, the OPERATING indicator illuminates, indicating that the equipment is in operation. If there is an abnormal condition in the equipment because of the position of one of the test switches, the ABNORMAL CONDITION indicator is illuminated. There is another ABNORMAL CONDITION indicator in the Test Switch Group. It is not possible to start the equipment in the NORMAL mode if there is an abnormal condition present.

Before the computer is started it is important that the MASTER CLEAR button be pressed. This clears all flip-flops except the X Register, sets the Program Address Counter to 40000, and sets the Main Pulse Distributor to MP 6.

The STEP button is used in the TEST mode in conjunction with the MANUAL STEP selections made in the Operating Rate Group. Pressing the FORCE STOP button any time the system is in operation causes the system to stop and illuminate the FORCE STOP indicator. This indicator remains illuminated until the computer is started again by pressing the START button or until the MASTER CLEAR button is pressed.

The EMERGENCY OFF button is used only in the case of extreme emergency. The pressing of this button opens the emergency off circuit. This removes all power from the equipment, including the blowers, magnetic drum, and timer circuit supply.

k. B FAULT GROUP. - Each B Fault in the equipment causes two of the indicators in this group to illuminate: the indicator of the specific fault and the B FAULT indicator. The IO fault, the MCT fault, and two of the MT faults (the NO INFORMATION FAULT and the SPROCKET ERROR fault) can be cleared by a master clear. Both the appropriate indicator and the B FAULT indicator extinguish when the MASTER CLEAR button is pressed.

The VOLTAGE fault, the MATRIX DRIVE fault, and the other two MT faults (the UNISERVO INTERLOCK fault and the SELECTION ERROR fault) require corrective maintenance to clear the fault. When the trouble is cleared, the individual fault indicator is extinguished and the B FAULT indicator can then be cleared by a master clear.

l. A FAULT GROUP. - The illumination of an indicator in this group indicates that one of the six A Faults has occurred. To clear the TEMP fault and the WATER fault, corrective maintenance is required. When the cause of the fault is corrected, the indicator is extinguished and the equipment can be started by pressing the START button in the Operating Group. The equipment can be started after any of the other A Faults by removing the cause of the fault

(if necessary), pressing the CLEAR A FAULT button, and then pressing the START button in the Operating Group.

m. TEST SWITCH GROUP. - This group consists of three indicators, two key-operated switches, and a number of toggle switches. To permit equipment operation in the NORMAL mode, all the toggle switches must be in the "down" position, except the AMPLIFIER MARGINAL CHECK SWITCHES which, because they are three-position switches, must be in the center position. The key switches must be in the OFF position. The ABNORMAL CONDITION indicator is automatically illuminated when any of these switches are not in the normal position.

Placing any of the switches in this group in the test position while the computer is operating in the NORMAL mode causes an Abnormal Condition fault and stops the computer until the switch is returned to the normal position. Computation can be resumed by pressing the START button. There are Normal relay contacts in all switch circuits so that their TEST mode function is disconnected. This prevents any damage to the program being run. This disconnected condition is not in effect if the computer is operating in the TEST mode; therefore, placing a switch in its test position places its function in effect.

The switches in this group are divided into 13 groups.

(1) DISCONNECT SWITCHES. - Four of these groups provide a means of disconnecting various circuits and are labelled as follows: DISCONNECT MD WRITE VOLTAGES, DISCONNECT CLEAR, DISCONNECT INITIATE WRITE, and DISCONNECT. When any of these switches are in the "up" position, the corresponding signal is interrupted. For example; placing the DISCONNECT WAIT INT. switch in the "up" position disconnects the WAIT INTERNAL signal from the Master Clock so that the advancing of the Main Pulse Distributor does not cease during an instruction subsequence.

(2) KEY SWITCHES. - The BY-PASS TEMPERATURE INTERLOCK indicator and key-operated switch are used to by-pass the A Fault temperature interlock circuit. If the switch is turned to the ON position, the indicator illuminates and a buzzer sounds continuously. This feature is used only in extreme cases, normally only when an important program is nearing completion and a temperature fault occurs.

The BY-PASS CABINET INTERLOCK indicator and key-operated switch are used to by-pass the cabinet door interlock system while maintenance is being accomplished in a cabinet. To operate in the NORMAL mode both of these switches must be in the OFF position.

(3) TEST-NORMAL SWITCH. - The TEST mode of operation can be selected by placing this switch in the "up" position. When TEST is selected in this manner, none of the lockouts on the set and clear buttons or the test switches is in effect.

(4) DRUM-OSCILLATOR SWITCH. - For NORMAL operation this switch is in the DRUM position and the 500kc timing pulses are supplied to the Master Clock by the Magnetic Drum. For test operations it is sometimes desirable to supply the timing pulses from an oscillator. Placing this switch in the OSCILLATOR position disconnects the Magnetic Drum source and supplies the timing pulses from a 500 kc oscillator.

(5) FORCE MC. - The FORCE MC switches are used to place all zeros and ones into the 36 MC matrices. With the FORCE ZEROS switch in the "up" position, the READ/RESTORE signal is prevented from restoring ones in the cores which held ones; thus after the first READ/RESTORE signal, all of the cores in the word referenced will store a "0". With the FORCE ONES switch in the "up" position, an enable is applied to amplifiers so that on each MCP 2 all Input Register flip-flops are set to "1". Each READ pulse will then read all ones in each MCS address referenced.

(6) MD NORMAL-ABNORMAL SWITCH. - This switch provides a means of selecting the reserve space on the Magnetic Drum. With this switch in the "up" position the MD location control circuits are altered so that the normal space on the drum is locked out and a reading operation can be performed in the reserve space. The MD write voltage is disconnected while the switch is in the "up" position to prevent the information in the reserve space from being destroyed.

(7) AMPLIFIER MARGINAL CHECK SWITCHES. - These switches are used to check tube conditions for MD, MT, PT and MC through a variation of grid bias. The HI-LO toggle switches are used to supply a higher-than-normal and a lower-than-normal grid bias to the selected MD, MT, PT or MC amplifier tubes.

(8) SELECT F_1 SWITCH. - In the normal "down" position this switch selects F_1 at MC address 00000. For test purposes it is possible to select F_1 at MD address 40001 by throwing the SELECT F_1 switch to the "up" position.

(9) REDUCE HEATER VOLTAGE SWITCHES. - The heater voltage of the tubes in the circuits of MD, MT, MC, the Arithmetic Section, and the Control Section can be reduced from 6.3vac to 5.7vac by these switches. This reduction in heater voltage is often sufficient to cause a weak tube to malfunction.

3. ARITHMETIC SECTION

These indicators and buttons are shown in Figure 3. The sequences occurring in the control flip-flops are listed in TIMING SEQUENCES under the Subcommand Timing Sequences, ASC, and ASC/SK heading; the operations in Q, A, and X during the execution of instructions are listed under the Command Timing Sequences heading.

a. ARITHMETIC SEQUENCE CONTROL. - This group consists of 24 pairs of indicator lamps, each vertical pair representing a flip-flop used in arithmetic sequencing. When set to "1", the flip-flops of the INIT. ARITHMETIC SEQUENCE group initiate the proper sequencing required to carry out arithmetic operations, e.g., Scale Factor, Divide, etc. The DIVIDE SEQUENCE flip-flops are used in performing divide operations. The PROBE group produces the required sequence of pulses to carry out the initiated sequences. Miscellaneous flip-flops shared by more than one arithmetic sequence are: DEL, ADD (Delay Add), SP, SUBT. (Split Subtract), OVERFLOW, REST. X (Restore X), MULT. STEP (Multiply Step), and EXT. SEQ. (Extend Sequence). One manual clear button is provided for test purposes. The state of these flip-flops during the various arithmetic sequences is shown in tabular form in Timing Sequences under the Arithmetic Sequence Control heading.

b. Q REGISTER. - The Q REGISTER indicator group, consisting of 36 pairs of lamps, is divided into 12 groups of three bits each. These are indicators for the 36-stage flip-flop Q register, used as a storage and shift register. One manual clear button and 36 manual set buttons are provided for test purposes.

c. ACCUMULATOR. - The ACCUMULATOR indicator group, consisting of 72 pairs of lamps, is divided into 24 groups of three bits each. This register is a 72-stage flip-flop system having accumulative and shifting properties. It is used to add, subtract, or shift 72-bit extensions of 36-bit numbers. Manual set buttons are provided for each stage for the purpose of testing. One manual clear button is provided for each half (A_L and A_R) of the Accumulator.

d. X REGISTER. - The X REGISTER indicator group consists of 36 pairs of indicators, divided into 12 groups of three bits each. These are indicators for the X Register, which serves as a temporary storage for 36-bit words in transit between Q, A, MC, MD, IOB, and for words used in certain arithmetic operations. For example, during division, X contains the divisor. The six lower-order stages of X serve as a 6-bit exchange register for the typewriter and high speed punch. The eight lower-order stages serve as an 8-bit exchange register for IOA. One manual clear button and 36 manual set buttons are provided for test purposes.

4. CONTROL SECTION

These indicators and buttons are shown in Figure 3. The sequences occurring in the flip-flops and translators are listed in Timing Sequences under the following headings:

Command Timing Sequences:

Loading Instructions
Instruction Reference Commands
Program Instructions

Subcommand Timing Sequences:

Storage Class Control, SCC
Arithmetic Register Access Control, ARAC
Repeat Sequence Control, RSC

a. MASTER CLOCK. - The MASTER CLOCK indicators consist of four pairs of lamps labelled CSS (Clock Source Selector) I, CSS II, CRS (Clock Rate Control) I, and CRC II. The CSS I and CSS II flip-flops control the selection of either the magnetic drum or oscillator as a source of clock pulses. If CSS I is set to "0", CSS II is also set to "0" after a short delay, and the 500kc oscillator is selected as a source of CLOCK PULSES. With CSS I and CSS II set to "1", the magnetic drum is selected as a source of CLOCK PULSES. With CRC I and CRC II flip-flops set to "1", CLOCK PULSES are interrupted, stopping the equipment operation. With CRC I and CRC II set to "0", CONTROLLED CLOCK PULSES are allowed to pass and the operation of the equipment is resumed.

b. PULSE DISTRIBUTION CONTROL. - This group consists of six pairs of indicators labelled HPC (High-Speed Punch Control), TWC (Typewriter Control), WAIT INTERNAL, WAIT EXTERNAL, WAIT RSC (Repeat Sequence Control) and STOP. The HPC flip-flop indicates a "1" when a high-speed punch operation is initiated. If another high-speed punch operation is initiated before the previous operation has been completed, MPD is stopped until the HPC flip-flop is again set to "0". If a typewriter operation has been initiated, the TWC flip-flop indicates "1". This condition is maintained until the current operation has been completed. The WAIT INTERNAL flip-flop is set to "1" when a read or write reference is made to MD, MC, or the Q REGISTER, preventing the advancement of MPD until the reading or writing operation has been completed. When a second print or punch reference is made, and a previous reference to the referenced unit has not been completed, the WAIT EXTERNAL flip-flop is set to "1". This prevents the second operation from starting until the first is completed. During repeated instructions each execution of the Repeat (75 jnw) instruction sets the WAIT RSC flip-flop to "1". This prevents MPD from advancing while certain Repeat Sequence Control operations are being performed. When the repeated instructions have been completed the WAIT RSC flip-flop is set to "0". When initiating an equipment stop, the STOP flip-flop within this group will be set to "1", which prevents MPD from advancing. One manual clear button is provided, at the right of the PULSE DISTRIBUTION CONTROL indicators, which may be used to clear all flip-flops in this group to "0". Individual manual clear buttons are provided for HPC and TWC.

c. MPD. - The MPD (Main Pulse Distributor) group consists of three pairs of lamps which indicate the state of the flip-flops of a three-stage binary counter. When this binary counter is advanced, it produces a cycle of 4, 5, 6, 7, or 8 pulses, depending upon the particular instruction being executed. MPD is advanced intermittently by pulses from the Pulse Distributor Control.

d. MAIN PULSE DISTRIBUTOR. - The MAIN PULSE DISTRIBUTOR consists of eight indicator lamps numbered 0 through 7. These lights provide an indication of the translated count produced by the MPD flip-flops. For example, when the 5 lamp in this group is glowing, the next pulse to be produced by MPD is MP 5. One manual set button is provided for each indicator of this group.

e. PROGRAM CONTROL REGISTER. - The PROGRAM CONTROL REGISTER group consists of the MAIN CONTROL REGISTER, MCR, the U ADDRESS COUNTER, UAK, and the V ADDRESS COUNTER, VAK. During the execution of an instruction, a 36-bit instruction word is contained in these registers.

MCR consists of six flip-flops capable of storing a two-digit (octal) operation code, which represents the type of instruction to be executed. For example, if the contents of MCR are 001001 binary (11 octal), a Transmit Positive (Operation Code 11) instruction is executed. One manual clear and six manual set buttons are provided for test purposes.

The 15-stage U ADDRESS COUNTER functions as both a register and a counter. When repeated instructions are executed following a Repeat (75jnw) instruction, the contents of UAK may be advanced by one count after each instruction, making each repeated execution different from the last. The contents of UAK may be interpreted in various ways, depending upon the particular instruction being executed. During some instructions, the left-hand three bits of UAK form a

j octal digit 0, 1, 2, or 3, and the right-hand 12 bits form a four-digit octal value n. For example, during an External Function (17-v) instruction a j value of 1 signifies that IOB is used rather than IOA. During other instructions, UAK contains a u execution address of five octal digits. For example, during a Transmit Positive (1luv) instruction, a word is read from storage address u. One manual clear and 15 manual set buttons are provided for test purposes.

The 15-stage V ADDRESS COUNTER functions both as a register and a counter. When repeated instructions are executed following a Repeat (75jnw) instruction, the contents of VAK may be advanced by one count after each execution. During most instructions, VAK contains a five octal digit v execution address. During some instructions, VAK contains a k value used to signify that a certain number of shifting operations are to be carried out during the instruction. One manual clear and 15 manual set buttons are provided for test purposes.

f. MAIN CONTROL TRANSLATOR. - This group consists of 57 lamps which indicate the translated contents of the MCR stages 0 through 5. Although 64 different combinations of "1" and "0" can be present in MCR, only 57 of these are acceptable combinations and are so indicated within the MAIN CONTROL TRANSLATOR group. The primary function of the MAIN CONTROL TRANSLATOR group is to indicate the translated six-bit binary contents of MCR, which show the type of instruction being executed. For example, if the content of MCR is binary 001001, the 11 indicator in the MAIN CONTROL TRANSLATOR group glows while a Transmit Positive (1luv) instruction is executed.

g. J TRANSLATOR. - This group consists of four lamps that indicate the translated contents of U ADDRESS COUNTER stages 12 and 13.

h. STORAGE ADDRESS REGISTER. - This group consists of 15 pairs of lamps that indicate the contents of the 15-stage STORAGE ADDRESS REGISTER. This register temporarily stores execution addresses obtained from UAK and VAK. When a read or write reference is made to A, Q, MC, or MD, the address to be read or altered is stored in SAR. Also, the lower-order seven stages of SAR function as the Shift Counter, SK. When shifting is to be performed in A or Q, the Shift Counter is used to count the number of shifting operations to be performed. One manual clear and 15 manual set buttons are provided for test purposes.

i. SCC TRANSLATOR. - When a read or write reference is made to a storage address, the A indicator in this group is illuminated if the address in the STORAGE ADDRESS REGISTER begins with 32 through 37 (octal). The Q indicator is illuminated if the address begins with 31, and the MD indicator is illuminated if the address begins with 4, 5, 6, or 7. The MC indicator glows if the first octal digit of the address is 0, and the NOT MC indicator is illuminated for all other addresses in SAR.

j. SK TRANSLATOR. - The right-hand seven stages of the STORAGE ADDRESS REGISTER are used as a shift counter which count each shift operation performed in A or Q. The translated content of the STORAGE ADDRESS REGISTER is indicated in the SK TRANSLATOR group when the contents of SK are 38, 1, 0 or NOT 0.

k. PROGRAM ADDRESS COUNTER. - This group consists of 15 pairs of lamps which indicate the contents of the 15-stage PROGRAM ADDRESS COUNTER, PAK.

This counter serves a dual purpose: 1) preceding each instruction sequence, the address of the instruction to be executed is obtained from PAK, 2) during a repeated instruction, PAK contains a repeat count used to determine the number of times the repeated instruction is executed. During each instruction sequence, if no program jumps occur, PAK is advanced by one count so that instructions stored at consecutive addresses are executed. When a program jump occurs, PAK is altered to a new address, then normal operation resumes. One manual clear and 15 manual set buttons are provided for test purposes.

1. FAULTS, REPEAT SEQUENCE CONTROL AND STORAGE CLASS CONTROL. - This group consists of 21 pairs of flip-flop indicators, divided into three sub-groups. When an SCC, MCT, or DIV (Divide) fault occurs within the equipment, the corresponding FAULTS indicator shows a "1". This condition energizes relays that illuminate an indicator in either the A Fault Group or the B Fault Group on the center switch panel and produce an A or B Fault stop. Each flip-flop indicated in the FAULT group is provided with one manual clear button for test purposes.

The A ZERO flip-flop indicators show a "1" when a Subtract 1 from A sequence is executed and the contents of A become "0". The "1" enable from this flip-flop produces special enables in the Main Control Translator for instructions 43 and 47. After each instruction has been completed the flip-flop is reset to "0". This flip-flop is provided with one manual set button.

The REPEAT SEQUENCE CONTROL group consists of eight pairs of indicators, labelled 75, HOLD RPT., JUMP TERM., INIT. RPT., INIT. TEST, END RPT. DELAY TEST, and ADV. ADD. The flip-flops indicated by this group perform operations for execution of repeated instructions. During a Repeat (75jnw) instruction, the 75 flip-flop is set to "1" to produce a special enable used in CTC. This flip-flop is reset to "0" when a repeat sequence is started. The HOLD RPT. flip-flop is set to "1" during a 75 instruction and causes the next "repeated" instruction to be held in MCR, UAK, and VAK while it is being repeated. The JUMP TERM. flip-flop is set to "1" during a repeated jump instruction when a jump condition occurs. This causes the repeated instruction to be terminated and the jump to be executed. The INIT. RPT. flip-flop is set to "1" during a Repeat (75) instruction to start the repeat sequence. INIT. TEST is set to "1" after each repeated instruction execution. If less than the proper number of executions have taken place, this flip-flop is cleared to "0". The END RPT. flip-flop is set to "1" during the 75 instruction sequence. This condition causes the next instruction to be repeated and UAK and VAK to be advanced conditionally. When the proper number of repeated executions has occurred, this flip-flop is cleared to "0". The DELAY TEST flip-flop produces a delayed pulse two microseconds after the INIT. TEST flip-flop has been set to "1". This pulse is used to terminate each repeated instruction execution. The ADV. ADD. flip-flop is set to "1", if no jump has occurred, after each repeated instruction execution. When set to "1", this flip-flop causes UAK and VAK to be conditionally advanced.

The STORAGE CLASS CONTROL group consists of seven pairs of indicators labelled INIT. READ, INIT. WRITE, IW (0-14), IW (15-29), READ Q, WRITE A OR Q, and CLEAR A. The flip-flops indicated by this group control reading and writing operations in A, Q, MC, and MD. If a 36-bit word stored in A, Q, MC, or MD, is to be read, the INIT. READ flip-flop is set to "1". The next CONTROLLED CLOCK PULSE clears the INIT. READ flip-flop to "0" and initiates a reading

operation in A, Q, MC, or MD, depending upon the address in SAR. If a 36-bit word is to be written in A, Q, MC or MD, the INIT. WRITE flip-flop is set to "1". The next CONTROLLED CLOCK PULSE clears the INIT. WRITE flip-flop to "0" and initiates a writing operation in A, Q, MC, or MD. The INIT. WRITE (0-14) flip-flop is set to "1" when the v address portion of a word is to be written in MC or MD. The next CONTROLLED CLOCK PULSE clears this flip-flop to "0" and initiates the proper writing operation in MC or MD. The INIT. WRITE (15-29) flip-flop is set to "1" when the u address portion of a word is to be written in MC or MD. The next CONTROLLED CLOCK PULSE clears this flip-flop to "0" and initiates the proper writing operation in MC or MD. If a 36-bit word is to be read from Q to the X Register, the READ Q flip-flop is set to "1". The next CONTROLLED CLOCK PULSE clears this flip-flop to "0" and produces signals that transmit the contents of the Q Register to the X Register. The WRITE A OR Q flip-flop is set to "1" when a word is to be transmitted from X to Q, or from X to the right half of the Accumulator, A_R. The next CONTROLLED CLOCK PULSE clears this flip-flop to "0" and either initiates the adding of X to A or transmits X to Q, depending upon the address in SAR. When the Accumulator is to be cleared to zero, the CLEAR A flip-flop is set to "1". The next CONTROLLED CLOCK PULSE clears this flip-flop and continually clears either A_R or A_R and A_L, depending upon the particular instruction being executed and the contents of SAR.

m. PROGRAM INTERRUPT. - This group consists of indicators for the Initiate flip-flop, labelled INIT., and the Interrupt flip-flop, labelled INTERRUPT. These flip-flops are used with either a manual interrupt or an interrupt from external equipment. A set button is provided for the Initiate flip-flop and a clear button is provided which clears both flip-flops.

5. MAGNETIC CORE STORAGE CONTROL.

This section is shown in Figure 4. The sequences occurring in the flip-flops are listed in TIMING SEQUENCES under the Subcommand Timing Sequences, MCAC heading.

a. MC INPUT REGISTER. - When a write reference is made to MCS, these flip-flops temporarily store the 36-bit word being written in MCS. When a word is being read, this register holds the word until it is re-written. One manual clear and 36 manual set buttons are provided for test purposes.

b. MC ADDRESS REGISTER. - This 12-stage register stores the MC address which determines the X and Y coordinates used to address or select a given core within each of the 36 matrices. When a read or write reference is made to MCS, these flip-flop settings are obtained from SAR. One manual clear and 12 manual set buttons are provided for test purposes.

c. MC CONTROL FLIP-FLOPS. - The MON INT (Monitor Intensity) flip-flop is set to "1" each time a read or write reference is made to MCS. While in the "1" state, a pulse is applied to the grid of the monitor tube, which in turn produces a bright spot in one of 4096 positions on the screen of the cathode-ray tube. The exact location of this illuminized spot is determined by the address being read from, or written into, MCS. During a read or write sequence, the R/W ENABLE (Read Write Enable) flip-flop is set to "1" for 8.6 microseconds and is used in forming CLEAR/READ PULSES. These pulses read the content of one

MC address to the Input Register and leave each bit of the address in the "0" state. A WRITE/RESTORE pulse is formed next, which either restores the address to its initial value or writes a new word into the address. The READ PULSE flip-flop is set to "1" during the first half of a read or write sequence and produces the CLEAR/READ pulse. Four microseconds later the WRITE PULSE flip-flop is also set to "0". During the last half of the read or write sequdnce, the ENAB I-D (Enable Inhibit-Disturb) flip-flop is set to one for 3.4 microseconds. This produces an enabling pulse that conditionally inhibits the writing of "1's" in the magnetic cores during the write or restore sequence. This condition also permits a DISTURB pulse to be applied to the magnetic cores. The DISTURB pulse is applied to all cores, returning them to a standard flux density that is relatively insensitive to half magnitude pulses applied in either direction. When the W/R (Write/Restore) flip-flops are set to "1" a 36-bit word, contained in the cores, is transmitted to the X Register. With the W/R 0-14 (Write/Restore 0-14) flip-flop set to "0", digits 0 through 14 of the currently-sampled MCS word are restored to "1" if "1's" were read out. With this flip-flop set to "1", new information from the X Register is written into MCS. The function of the 15-29 and 30-35 flip-flops is similar to that described for W/R 0-14, except that these operate on digits 15 through 29 and 30 through 35, respectively. If writing is to be done in all 36 digit positions, all three W/R flip-flops are set to "1".

d. MC PULSE DISTRIBUTOR. - The Magnetic Core Pulse Distributor indicators show the translated contents of the three-stage binary counter located at the immediate right and labelled III, II and I. For example, when the 2 indicator is glowing, the next CONTROL pulse to be produced is MCP 2.

6. MAGNETIC DRUM STORAGE CONTROL

These indicators and buttons are shown on Figure 4. The timing sequences for the flip-flops indicated by these lights are listed in Timing Sequences under the Subcommand Timing Sequences, MDAC heading.

a. GS. - These two pairs of indicators provide indication for the two-stage Group Selector. The Magnetic Drum contains four sets of read-write heads capable of reading or writing in four different "groups" of tracks on the drum. These are designated Groups 4, 5, 6, and 7. When a read or write reference is made to the Magnetic Drum system, the content of this register is 00, 01, 10, or 11 (binary), corresponding to MD group 4, 5, 6, or 7, respectively.

b. MD GROUP. - The translated contents of the two Group Selector flip-flops are indicated by MD GROUP indicator 4, 5, 6, or 7.

c. MD ANGULAR INDEX COUNTER. - This group provides indication for the 12-stage binary counter AIK that registers the number of pulses read from the timing track of the magnetic drum. The instantaneous count in this register represents the angular position of the drum and is used in locating storage positions on the drum. One manual clear and one manual set button are provided for test purposes.

d. MD INTERLACE. - These 5 indicators provide an indication of which interlace is being used. There are interlace chassis for a 4, 8, 16, 32, or 64 interlace, and the chassis providing the desired interlace is plugged into jack 60061. A spare chassis, that can be used to provide a 1 interlace, is provided.

e. MD CONTROL FLIP-FLOP INDICATORS. - This group consists of 13 pairs of indicators, which provide indication for the Magnetic Drum Access Control flip-flops. The INIT WRITE flip-flop is set to "1" when a 36-bit word is to be written in a MD storage position. This condition initiates the writing sequence that clears this flip-flop to "0". The function of the INIT WRITE (0-14) flip-flop is similar to INIT WRITE (above), but is used only when the v address portion of a word is to be written. The INIT WRITE (15-29) flip-flop is set to "1" when the u address portion of a word is to be written in an MD storage position. This condition initiates the writing sequence that clears this flip-flop to "0". When a 36-bit word is to be read from the drum, the INIT READ flip-flop is set to "1", initiating the read sequence that clears this flip-flop to the "0" state.

The INIT DELAYED READ flip-flop is set to "1" when a 36-bit word is to be read from the drum and when the drum has been operating upon a group other than the one currently specified by SAR; therefore, the read sequence is delayed to provide additional time for group switching. During the delay this flip-flop is cleared to "0". The READ LOCKOUT I, II, and III group indicates a three-stage binary counter that is set to binary 100 after the INIT DELAYED READ flip-flop has been set to "1". The count is advanced, and, when the count is equal to binary 000, the reading operation is started. This provides a delay of about 32 microseconds, which is required for changing the MD group selection circuits. In the MD normal mode of operation, the COINC. LOCKOUT flip-flop is cleared to "0" while AIK counts 0 through 4095, allowing a read or write sequence to occur only in the 4096 storage positions of each drum track group. With each revolution of the drum, the MARK PULSE read from the control track sets the PRESET flip-flop to "1". The next control pulse presets AIK to "ones" and clears the PRESET flip-flop to "0". The ADVANCE AIK flip-flop is set to "0" during a read sequence. During a write sequence it is set to "1", slightly delaying the advancement of AIK. This synchronizes the system to the writing operation.

When the MD Abnormal mode has been selected, the COINC. LOCKOUT flip-flop is set to "1" while the normal portion of the drum is passing under the read-write heads and is cleared to "0" at the beginning of the reserve space. This allows the Coincidence Detector circuitry to operate in the reserve space. Only a reading operation can be performed when the computer is operating in the MD Abnormal mode, because the MD write voltage is disconnected by contacts of the MD Abnormal relay K60002.

The CPD I and CPD II flip-flops make up a two-stage binary counter. This counter is used to produce a series of three clock pulses, which control the MD read and write sequences. This distributor operates from 500kc CLOCK PULSES produced from 125kc TIMING PULSES by a multiplier circuit.

7. HIGH-SPEED PUNCH REGISTER

These seven indicators show the contents of the seven-stage High-Speed Punch (thyratron) Register. When a high-speed punching operation is initiated, the six-hole combination to be punched in tape levels 1 through 6 is transmitted from X into stages 0 through 5 of this register. If a seventh-level hole is also to be punched, stage 6 is lit. When punching is completed in one frame of tape, the HS PUNCH REGISTER thyratrons and their indicators extinguish.

8. HIGH-SPEED PUNCH

This group consists of two pairs of indicators that show the states of the two flip-flops used to control the high-speed punching operation. When a high-speed punching operation is to be executed, the INIT flip-flop is set to "1". If the High-Speed Punch drive motor is running, the next closure of a sync contact in the punch causes the contents of the HS PUNCH REGISTER to be reproduced on punched tape and clears the INIT flip-flop to "0". During the punching operation, the pulse from a sync contact in the punch sets the RES (Resume) flip-flop to "1". This condition produces a resume signal for the operation and clears this flip-flop to "0".

9. TYPEWRITER REGISTER

These seven indicators show the contents of the seven-stage thyratron Typewriter Register. When a typewriter operation is initiated, a 6-bit combination is transmitted from X to stages 0 through 5 of this register. The typewriter prints a character represented by the six-bit code. As each printing operation is started, a signal extinguishes the register thyratrons. One manual clear button is provided for test purposes.

10. INPUT-OUTPUT INDICATORS

These indicators and buttons, shown in Figure 2, are located on the left indicator panel and the left switch panel.

a. IOB. - The IOB group consists of 36 pairs of indicators that show the contents of the 36-stage IOB Register, which is an input and output register used in the execution of External Function (17-v) instructions, External Read (76jv), and External Write (77jv) instructions having j factors equal to 1. One manual clear button and 36 manual set buttons are provided for test purposes.

b. IOA. - The IOA group consists of eight pairs of indicators showing the contents of the eight-stage IOA Register, which is an input and output register used in the execution of External Read (76jv) and External Write (77jv) instructions having j factors equal to 0. One manual clear button and eight manual set buttons are provided for test purposes.

c. FAULTS. - This group consists of four indicators, each relating to an Input-Output Fault.

(1) IOA 1 FAULT. - This fault is indicated when the external control calls for a read operation from IOA into the computer before the data from the previous read operation has been assimilated by the computer.

(2) IOA 2 FAULT. - This fault is indicated when the external control calls for a read operation into IOA before the data from the previous write operation has been assimilated by the external equipment.

(3) IOB 1 FAULT. - This fault is indicated when the external control calls for a read operation from IOB into the computer before the data from the previous read operation has been assimilated by the computer.

(4) IOB 2 FAULT. - This fault is indicated when the external control calls for a read operation into IOB before the data from the previous write or select operation has been assimilated by the external equipment.

d. WAIT CONTROL. - This group consists of four pairs of indicator lamps. Four manual set buttons are provided for test purposes.

(1) IOA READ. - A "1" indicated by IOA READ means that the external equipment has sent information to IOA and allows the computer to assimilate the information. A "0" indication means that the external equipment has not completed sending information to IOA, and the computer will wait until the external equipment has completed its transmission to IOA before starting the next reading operation from IOA.

(2) IOB READ. - A "1" indicated by IOB READ means that the external equipment has sent information to IOB and allows the computer to assimilate the information. A "0" indication means that the external equipment has not completed sending information to IOB, and the computer will wait until the external equipment has completed its transmission to IOB before starting the next reading operation from IOB.

(3) IOA WRITE. - A "1" indicated by IOA WRITE means that the computer has transmitted data into the IOA Register. A "0" indication means that the external equipment has assimilated the data from IOA. If the external equipment has not completed this operation, the computer will wait before starting the next write operation.

(4) IOB WRITE. - A "1" indicated by IOB WRITE means that the computer has transmitted data into the IOB Register. A "0" indication means that the external equipment has assimilated the data from IOB. If the external equipment has not completed this operation, the computer will wait before starting the next write operation.

e. WRITE AND SELECT. - This group consists of three pairs of indicator lamps. Three manual set buttons are provided for test purposes.

(1) IOA WRITE. - A "1" indicated by IOA WRITE means that write data has been accepted by IOA from the computer. The presence of the "1" initiates writing operations in the external equipment.

(2) IOB WRITE. - A "1" indicated by IOB WRITE means that write data has been accepted by IOB from the computer. The presence of the "1" initiates writing operations in the external equipment.

(3) SELECT. - A "1" indicated by SELECT means that selection data has been accepted into IOB from the computer. The presence of the "1" initiates the setting-up of a mode of operation in a particular external equipment.

11. MONITOR UNIT

The Address Monitor is a five-inch cathode ray tube located directly above the central section of the Supervisory Control Panel. This tube produces a visible display of the addresses (cells) being referred to in MC. Storage

addresses in MC consist of 4096 positions, and are displayed by illuminated patterns that appear within the 64 x 64 raster of the Address Monitor.

A spot appearing in the upper left-hand corner of the raster represents MC address 00000 (octal), and a spot in the lower right-hand corner represents the MC address 07777 (octal). The deflection voltages, used to position the beams of the MC Monitor Unit, are obtained from the Deflection Generator in the MC Storage Section which converts the binary address in the MC Address Register to the proper deflection voltages for the monitor tube.

MANUAL INSERTION OF PROGRAMS

1. GENERAL

When it is necessary to alter an existing program in storage or to insert a new program into storage without using the photoelectric tape reader, a manual procedure is used to enter the new storage words via the Q Register. A similar type of procedure provides means for inspecting the contents of any chosen storage register by transmitting its contents into the Q Register so that the word may be observed on the Q Register indicators.

2. MANUAL WRITING FROM THE Q REGISTER

This is done in the following manner:

Step 1. Select MASTER CLEAR

Step 2. Select MANUAL STEP OPERATION

Step 3. Set MPD to 0

Step 4. Set MCR to 75 (Repeat)

Step 5. Set UAK to 50000 (set j to 5)

Step 6. Set VAK to 00000

Step 7. Press the START button

Step 8. Press the STEP button

Steps 2 through 8 set up an unterminated Repeat sequence. Since j is 5, only the v address is advanced at the end of each storage reference.

Step 9. Clear PCR (Clear MCR, UAK and VAK)

Step 10. Set MCR to 11 (Transmit Positive)

Step 11. Set UAK to 31000 (Q address)

Step 12. Set VAK to first address to be written into

Step 13. Set up the word to be written in the Q Register

Step 14. Press the STEP button

Step 15. Clear the Q Register

Steps 10 through 14 manually enter the word set up in Q at the selected v address. To continue writing in consecutive addresses, repeat steps 13, 14,

and 15 for each word to be written. If only a single word is to be written, steps 4 through 9 and step 15 may be omitted, since a Repeat operation is not needed.

3. MANUAL READING TO THE Q REGISTER

This is done in the following manner:

Step 1. Select MASTER CLEAR

Step 2. Select MANUAL OPERATION STEP

Step 3. Set MPD to 0

Step 4. Set MCR to 75 (Repeat)

Step 5. Set UAK to 60000 (set j to 6)

Step 6. Set VAK to 00000

Step 7. Press the START button

Step 8. Press the STEP button

Steps 4 through 8 set up an unterminated Repeat Sequence. Since j is 6, only the u address will be advanced at the end of each storage reference.

Step 9. Clear PCR (Clear MCR, UAK, and VAK)

Step 10. Set MCR to 11 (Transmit Positive)

Step 11. Set UAK to address of first word to be read

Step 12. Set VAK to 31000 (Q address)

Step 13. Press the STEP button

Steps 10 through 13 manually read the word at the selected u address to the Q Register where it is displayed for observation. Each time the STEP button is pressed a word from a consecutive u address will be displayed in Q. If only a single word is to be read, steps 4 through 9 can be omitted since a Repeat operation is not needed.

4. PROGRAM CORRECTION

If, while reading to the Q Register, an incorrect word is noted, the following steps should be followed to insert the correct word. (This procedure can be used whether or not a Repeat sequence is being used in the manual reading.)

Step 1. Clear Q

Step 2. Clear UAK and VAK

Step 3. Set UAK to 31000 (Q address)

Step 4. Set VAK to address to be written into

Step 5. Set up word to be written in the Q Register

Step 6. Press the STEP button

Steps 1 through 6 enter the correct instruction. To return to reading:

Step 7. Clear UAK and VAK

Step 8. Set UAK to the next address to be read from

Step 9. Set VAK to 31000 (Q address)

Step 10. Press the STEP button

Steps 7 through 10 return control to the manual reading procedure.

5. MANUAL BLOCK TRANSFER

To effect a manual block transfer from Magnetic Drum Storage to Magnetic Core Storage, the following steps should be performed.

Step 1. Select MASTER CLEAR

Step 2. Select MANUAL STEP OPERATION

Step 3. Set MPD to 0

Step 4. Set MCR to 75 (Repeat)

Step 5. Set UAK to 3n (set j to 3 and n to the number of words to be transferred)

Step 6. Set VAK to a w address containing a 56jv instruction

Step 7. Press the START button

Step 8. Press the STEP button

Steps 4 through 8 set up a terminated Repeat sequence. Since j is 3, both the u address and the v address will be advanced at the end of each storage reference.

Step 9. Press the FORCE STOP button

Step 10. Release MANUAL STEP OPERATION

Step 11. Clear PCR (Clear MCR, UAK and VAK)

Step 12. Set MCR to 11 (Transmit Positive)

Step 13. Set UAK to initial MD address

Step 14. Set VAK to initial MC address

Step 15. Press the START button

Steps 12 through 15, in conjunction with the Repeat, cause the block transfer of n words. Since address w contains a 56 instruction (Manually Selective Stop) and F_1 contains a 45 instruction (Manually Selective Jump) at the termination of the block transfer, control is transferred to F_1, from which a jump to the 56 instruction is effected, thus stopping the operation.

POWER SUPPLY SYSTEM MAINTENANCE

1. GENERAL

Maintenance of system power includes checking, resetting, or replacement of overload protection devices, checking and adjustment of equipment voltages, and locating and correcting power faults.

Where maintenance procedure requires admittance to the interior of cabinets, the door interlocks may be by-passed by operating the INTERLOCK BY-PASS switch on the Supervisory Control Panel.

2. CHECKING OVERLOAD PROTECTIVE DEVICES

The overload protective devices include the circuit breakers, overload relays, thermostats, manual reset switches, and overload fuses. Each element must be manually reset or, in the case of fuses, replaced.

a. CIRCUIT BREAKERS. - With the equipment power off, check for tripped circuit breakers at the following locations.

1) MOTOR ALTERNATOR CONTROL. - Alternator input breaker and alternator output breaker on the Alternator Control Panel and the five secondary breakers located inside the Alternator Control in the upper right hand corner.

2) POWER SUPPLY CABINET. - Circuit breakers on the 81300 unit at rear of the cabinet.

b. PROTECTIVE RELAYS. - Protective relays are located at the Motor Alternator Control inside the Magnetic Drum Storage Cabinet and the Cooling Cabinet. All are manually reset by pressing the associated reset plunger.

(1) ALTERNATOR CONTROL. - Power directional relay, instantaneous voltage relay and Frequency relay on the alternator control panel. Motor overload relays inside cabinet at lower left-hand corner.

(2) MAGNETIC DRUM STORAGE CABINET. - Motor overload starter control box adjacent to the drive motor.

(3) COOLING CABINET. - Motor overloads adjacent to motors.

c. SWITCHES. - Manual reset switches include the EMERGENCY OFF switch on the Supervisory Control Panel and the HIGH TEMPERATURE THERMOSTATS in the equipment Cabinets.

(1) SUPERVISORY CONTROL PANEL. - Press the EMERGENCY OFF to reset the switch.

(2) EQUIPMENT CABINET. - Press reset button adjacent to thermostat.

d. FUSES. - In most cases blown fuses may be located by observing the state of the BLOWN FUSE INDICATOR associated with the fuse. A glowing blown fuse indicator denotes a blown fuse. In specific cases where a fuse has no indicator associated with it, the fuse must be removed and checked with an Ohmmeter for electrical continuity. Fuse and indicator locations are listed in Table 1.

3. CHECKING POWER SUPPLY VOLTAGES

Power supply voltages are checked for proper values at the Power Control Panel. The procedure is as follows (Numbers in parentheses refer to numbers in Figure 1):

Step 1. Set the A-C SELECTOR SWITCH (1) to the position labelled with the voltage to be checked.

Step 2. Read the A-C VOLTMETER (2). The correct values are 220vac on each of the three phases and 110vac on the 110vac line.

Step 3. Set the D-C SELECTOR SWITCH (3) to the position labelled with the voltage to be checked.

Step 4. Read the D-C VOLTMETER (4). If the voltage value is correct, the needle of the meter will rest in the center of the white region of the scale.

4. ADJUSTING POWER SUPPLY VOLTAGES

Alternating current voltage is adjusted for proper value at the Alternator Control Panel, magnetically controlled d-c voltages are adjusted at the Power Control Panel, and Magnetic Core Storage bias voltages at the MC Bias Control Panel. The alternator output (a-c) and magnetic amplifier outputs (d-c) are easily adjusted by turning the appropriate adjusting knobs while observing the reading on the voltmeter. The MC bias voltages, however, are highly critical, and the optimum operating values are determined through the criteria established by the Magnetic Core Storage Test Routine.

a. ADJUSTING A-C VOLTAGES. - Adjustment of the a-c voltage is accomplished at the motor alternator control panel. The procedure is as follows.

Step 1. Observe the voltage value on the a-c meter on the right hand side of the Alternator Control Panel.

Step 2. While observing the meter, turn the a-c voltage rheostat until the meter reads 220vac.

b. ADJUSTING D-C VOLTAGES. - Direct current voltages are adjusted for proper value at the Power Control Panel. The procedure requires admittance to the cabinet interior. To gain admittance, by-pass the door interlocks by turning the BY-PASS INTERLOCKS switch on the Supervisory Control Panel. The procedure is as follows (Numbers in parentheses refer to numbers on Figure 1).

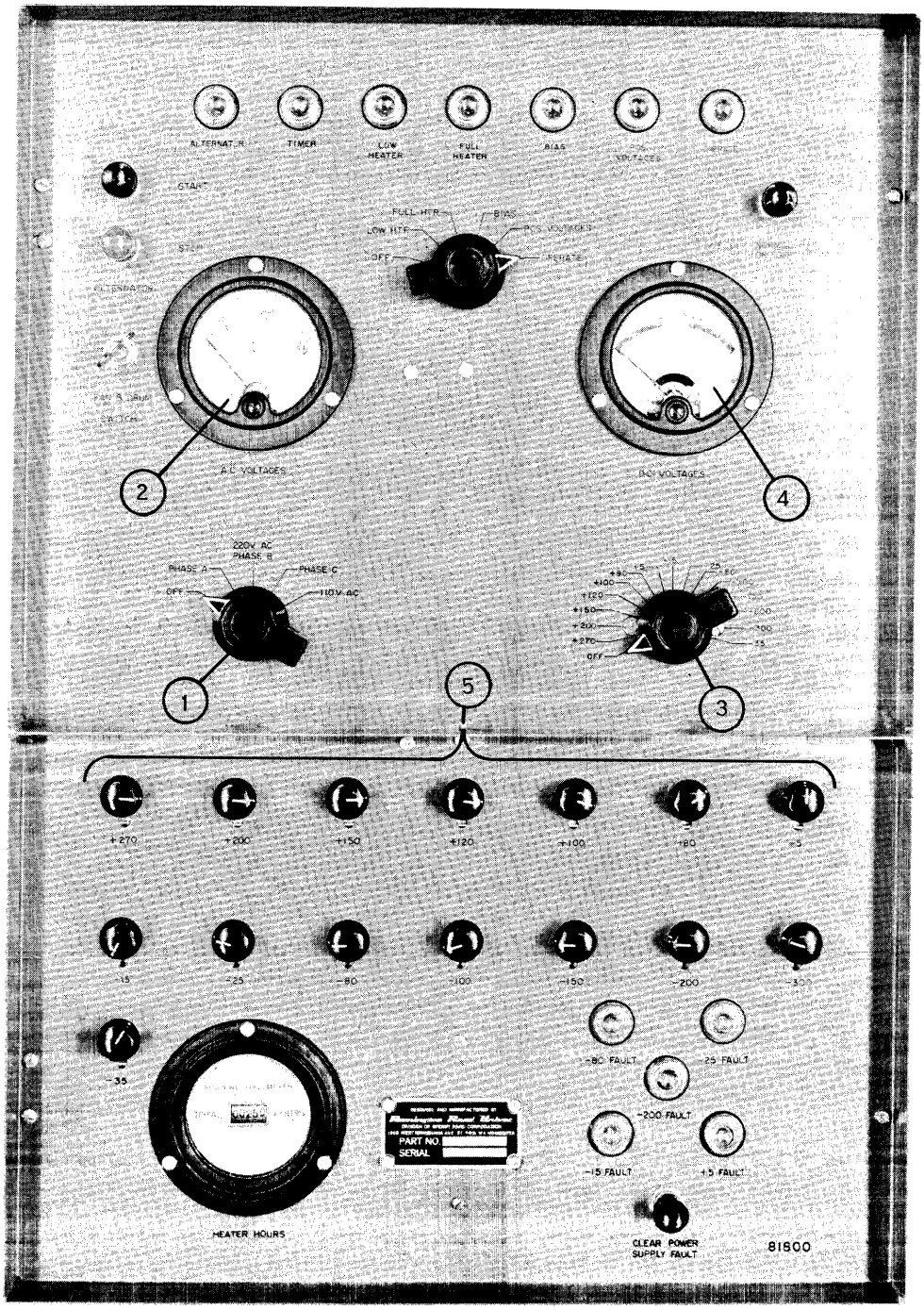


Figure 1. Power Control Panel
PX 134

Step 1. Set the D-C SELECTOR switch (3) to the position labelled with the voltage to be adjusted.

Step 2. Read the D-C VOLTMETER (4) while observing the voltmeter, turn the appropriately labelled adjusting knob (5) until the needle of the meter rests on the center line of the scale.

c. MAGNETIC CORE STORAGE ADJUSTMENT

(1) GENERAL. - The critical voltages for the Magnetic Core Storage Vacuum Tube Circuits are the SENSE BIAS, INHIBIT BIAS, and DRIVER BIAS. The adjustment controls for these voltages are located in the rear of the MC Cabinet. In general, the SENSE BIAS affects the circuit's ability to read from storage, the INHIBIT BIAS affects the circuit's ability to write into storage, and the DRIVER BIAS affects both reading and writing.

Two other types of controls are provided in the Magnetic Core Storage System. These are the individual Sense Amplifier Gain controls and the individual X and Y drive line current controls.

Each Sense Amplifier has a separate Sense Amplifier Gain control. Normally, this control does not require adjustment after the Magnetic Core Storage System has been placed in operation. However, if the SENSE BIAS and DRIVER BIAS adjustment fail to correct the trouble, the Sense Amplifier Gain control can be used. Sense Amplifier Gain controls are located on the 58800 units on front of the 50000 Cabinet.

Each X and Y core memory plane drive line has a separate current control rheostat. These drive line controls are adjusted for each individual drive line current output transformer. The final adjustment is made by the erection crew, and it should not be changed by maintenance personnel. The rheostat adjustments compensate for differences in transformer outputs and allow a high degree of uniformity in drive line currents.

A group of 12 toggle switches, located on the control panel in the rear of the MC (55000) cabinet, are used to turn each power supply voltage on or off. When these switches are used, the power can be turned off in the MC cabinet only. The use of these switches permits maintanance personnel to work on the MC cabinet while the rest of the computer is being operated.

(2) PRELIMINARY ADJUSTMENTS. - The preliminary adjustments are made to assure the proper generation and holding of "1's" and "0's" in storage. The procedure is as follows (Numbers in parentheses refer to corresponding numbers in Figure 2):

Step 1. Set the BIAS VOLTAGE selector switch (1) to SENSE BIAS.

Step 2. Observe the BIAS VOLTMETER (2).

Step 3. While observing the voltmeter, turn the SENSE BIAS control rheostat adjustment (3) until the meter reads approximately 14 volts d-c.

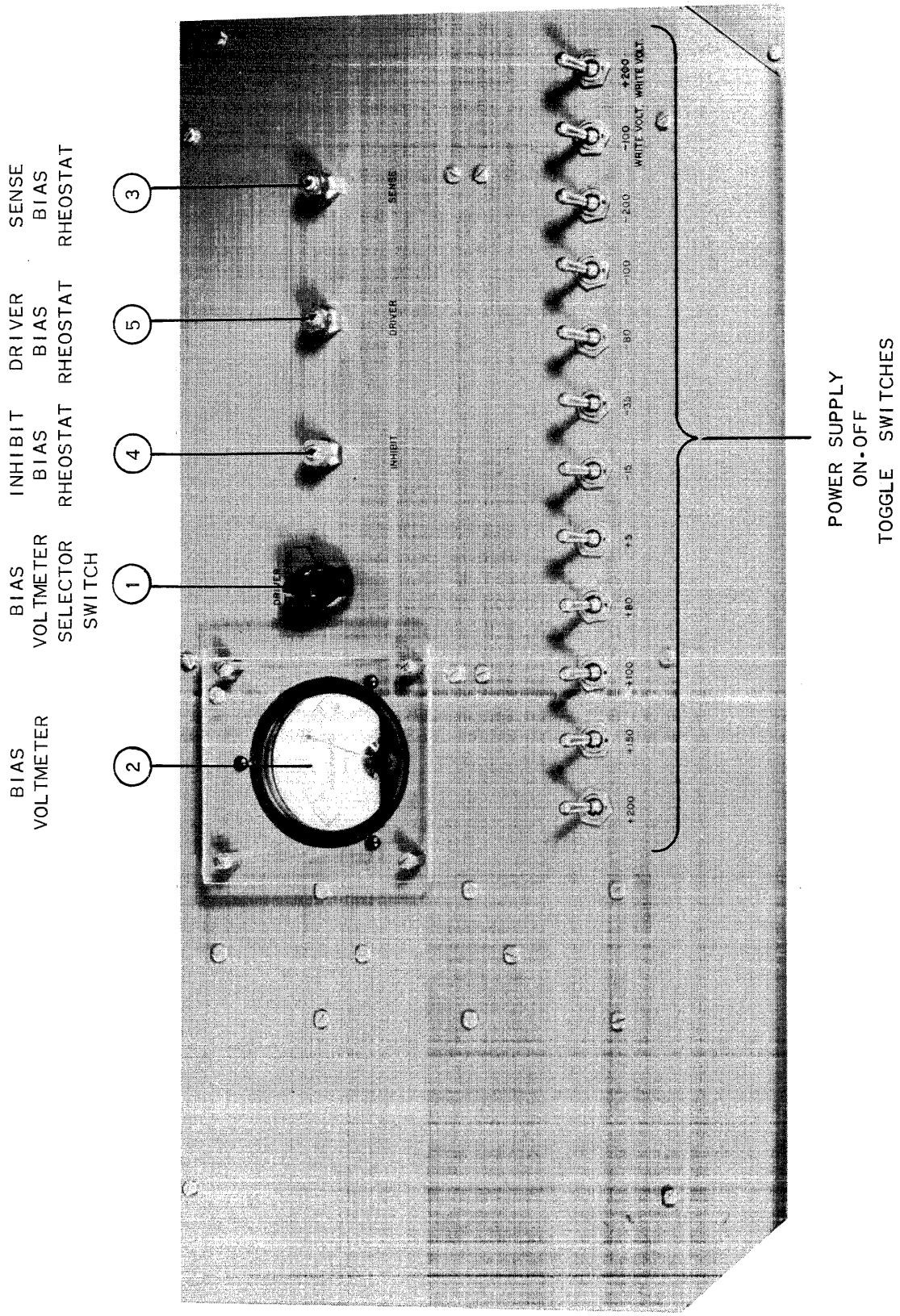


Figure 2. Power Supply Control Panel for MC Cabinet

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Step 4. Set the BIAS VOLTAGE selector switch (1) to INHIBIT BIAS.

Step 5. Observe the BIAS VOLTMETER (2).

Step 6. While observing the meter, turn the INHIBIT BIAS control rheostat (4) until the meter reads approximately 27 volts d-c.

Step 7. Set the BIAS VOLTAGE selector switch (1) to DRIVER BIAS.

Step 8. Observe the BIAS VOLTMETER (2).

Step 9. While observing the meter, turn the DRIVER BIAS control rheostat (5) until the meter reads 20 volts d-c.

Step 10. Set up an unterminated repeat transmit positive MC to Q reference.

Step 11. Set the FORCE ZERO switch on the SC Panel to the "up" position.

Step 12. Observe the Q Register with the disconnect clear Q switch in the "up" position; if any indicators record ones present, increase the SENSE BIAS slightly.

Step 13. Repeat steps 10, 11, and 12 until only "0's" are stored.

Step 14. Set the selector switch (1) to SENSE BIAS and observe the reading on the meter. The meter should read 14 volts d-c $\pm$ 3vdc. If the meter reads more than 17vdc, reset the SENSE BIAS to 14vdc, reduce the DRIVER BIAS to about 19.0vdc and repeat steps 10 through 14.

Step 15. Set the FORCE ONES switch on the SC Panel to the "up" position, and the Force Zeros switch to the down position.

Step 16. Set up an unterminated repeat transmit negative MC to Q reference.

Step 17. Observe the Q Register with the disconnect clear Q switch in the "up" position; if any indicators show the presence of "0's", reduce the SENSE BIAS slightly. If the system fails to write "1's", increase DRIVER BIAS to about 20.5vdc.

Step 18. Repeat steps 16 and 17 until only "1's" are stored.

Step 19. Set the selector switch to SENSE BIAS and observe the reading on the meter. The meter should read 14vdc $\pm$ 3vdc. If the meter reads less than 11vdc, reset the SENSE BIAS to 14vdc, increase the DRIVER BIAS to about 21vdc, and repeat steps 16 through 19.

Step 20. Return the FORCE ONES switch to the "down" position.

Step 21. Repeat steps 10 through 14. If further adjustments are made, repeat steps 16 through 21.

(3) FINAL ADJUSTMENT. - The criterion by which the final adjustments are made is the Magnetic Core Storage Test Routine. This routine, divided into eleven sections, checks the ability of the magnetic core memory system to read, write, restore, and hold information under marginal conditions. The severity of the test is dictated by the HI and LO amplifier marginal checks.

An adjustment of any one of the controlling factors, SENSE BIAS, INHIBIT BIAS, or DRIVER BIAS, may affect the other two. An adjustment for failure on one section of the test may affect the storage system in regard to the other tests. Thus, adjusting is done by testing, adjusting, and re-testing until the storage system passes the tests. A general procedure is described below.

When a test fails, the Flexowriter prints out the letter and other abbreviations denoting the test section that failed, the X and Y drive line numbers of the addresses on which it failed, and the digits of the addresses that failed. If the failures are in addresses in the same rows and/or columns in several digit planes, the fault is likely to be contained in the Driver circuits. If the errors are in one or more digit planes in addresses not related to each other, the fault is likely to be found in the Sense Amplifier (SENSE BIAS) or INHIBIT CIRCUIT. Therefore, by observing the pattern of failed addresses and digits, the malfunctioning circuit may be isolated and a trial adjustment may be made.

Run the MC test routine on each amplifier marginal check, noting which test portion failed on each margin, and adjust for each test in order. For example, if test A fails on one margin and test D on the other, adjust for test A, then re-run the test routine on each margin and adjust for failure of the next test in order.

(a) TEST A FAILED. - Failure on test A is generally due to an inferior sense signal.

1 If the failures are on several digits, decrease the SENSE BIAS slightly. If the failures are consistently on the same digit, increase the SENSE AMPLIFIER GAIN control for that digit. The inner adjustment varies the gain on the lower order bit. The outer adjustment varies the gain on the higher order bit.

2 Re-run the test on HI margin, decreasing the SENSE BIAS each time test A fails.

3 Run the test on LO margin. (An over adjustment for test A may cause test B to fail.)

(b) TEST B FAILED. - Failure on test B is generally due to an excessively large SENSE signal.

1 If the failures are on several digits, increase the SENSE BIAS slightly. If the failures are consistently on the same digit, decrease the SENSE AMPLIFIER GAIN control for that digit.

2 Re-run the test on LO margin, increasing the SENSE BIAS each time test B fails.

3 Run the test on HI margin. (An over adjustment for test B may cause test A to fail.)

If, by adjustment of SENSE BIAS, tests A and B cannot be made to pass on both margins, use the error type-out routine as a guide to determine if either the DRIVER BIAS or INHIBIT BIAS is at fault. If the same address or addresses repeatedly fail, or if the failing addresses are related by row or column, make a trial adjustment of the DRIVER BIAS in either direction and re-run the test. If the number of errors decrease, continue to adjust in the same direction; if the errors increase, adjust in the opposite direction.

If errors are in one or more digit planes in addresses not related to each other, make a trial adjustment of the INHIBIT BIAS. Re-run the test and observe an increase or decrease in the degree of error. Adjust accordingly.

(c) TEST D, E, F, G, H, OR J FAILED. - Failure of test D, E, F, G, H, or J may be caused by any of the three variables being slightly off in either direction, and must be corrected by trial and error. Use the error type-out as a guide in making adjustments.

1 If failures occur in the same address or addresses, or are related by rows and/or columns, make a trial adjustment of the DRIVER BIAS in either direction. Re-run the test and observe an increase or decrease in the degree of error. If the amount of errors decrease, adjust in the same direction; if the errors increase, adjust in the opposite direction.

2 If errors are in one or more digit planes in addresses not related to each other, make a trial adjustment of either the AMPLIFIER BIAS or INHIBIT BIAS, and repeat the test. If the amount of errors decreases, adjust in the same direction; if the amount of error increases, adjust in the opposite direction. If the errors increase regardless of the trial settings, return the adjustment control to the original position and repeat the trial adjustment with the other adjustment control.

3 If failures occur, run the test on all the marginal conditions employing the same adjustment procedure. Continue to run the test under alternate margins until the test checks out OK.

(d) TEST I FAILED. - Failure of test I may be due to excessive ripple or poor regulation of d-c voltages.

1 With the test program running, check the various d-c voltages with a scope for excessive ripple or poor voltage regulation.

2 Perform the necessary corrective measures and repeat the test.

(e) TEST K FAILED. - Failure of test K indicates faulty logical circuits.

1 Check flip-flop V21 and associated gates and crystals on the chassis in jack J55061 and J55071.

2 Check amplifiers V06, V08 and associated crystals on the chassis in jack J55061.

If errors persist and cannot be rectified by adjustment of voltages, replace the appropriate unit chassis in the DRIVER CIRCUIT, SENSE-INHIBIT circuit, or ACCESS CONTROL as deduced from the error type-out.

(4) TYPICAL OPERATING WAVEFORMS. - See Figures 3 through 6.

5. MOTOR ALTERNATOR MAINTENANCE

Maintenance procedures for the motor alternator are contained in the manufacturer's manual provided with the unit; refer to that manual for necessary information.

6. POWER UNIT CHASSIS MAINTENANCE

Unit chassis of the Power Supply System are rack mounted with external connections being provided by connector plugs or E-strips. Normally units of the power system are relatively trouble free; consequently, no spare units are provided. Minor maintenance such as replacing tubes or relays may be performed without removing the units from their racks. However, where a detailed circuit analysis is required, the malfunctioning unit may be removed by first uncoupling the connector and then removing the attaching screws.

a. MAGNETICALLY CONTROLLED D-C SUPPLIES (MAGNETIC AMPLIFIERS). - Trouble shooting usually requires removal of the power supply from the rack, however, prior to this, an investigation of circuit conditions at the output terminals may be beneficial. If the power supply does not operate with the load removed from the output terminals, the remedy for the failure probably requires removal of the unit from the rack.

(1) CONNECTING THE POWER SUPPLY FOR BENCH OPERATION:

Step 1. By means of changing jumper wires, connect the voltage control pot within the power supply into the circuit. See Figure 7, Jumper Connections for Internal and External pot.

Step 2. Connect 220vac, three phase, 60-cycle power through a switch to input terminals E01-1, 2, and 3. Connect the phase neutral to E01-5. Jumper E01-4 to E01-1, 2 or 3.

Step 3. Connect a d-c voltmeter to the output terminals, E01-6 and E01-7.

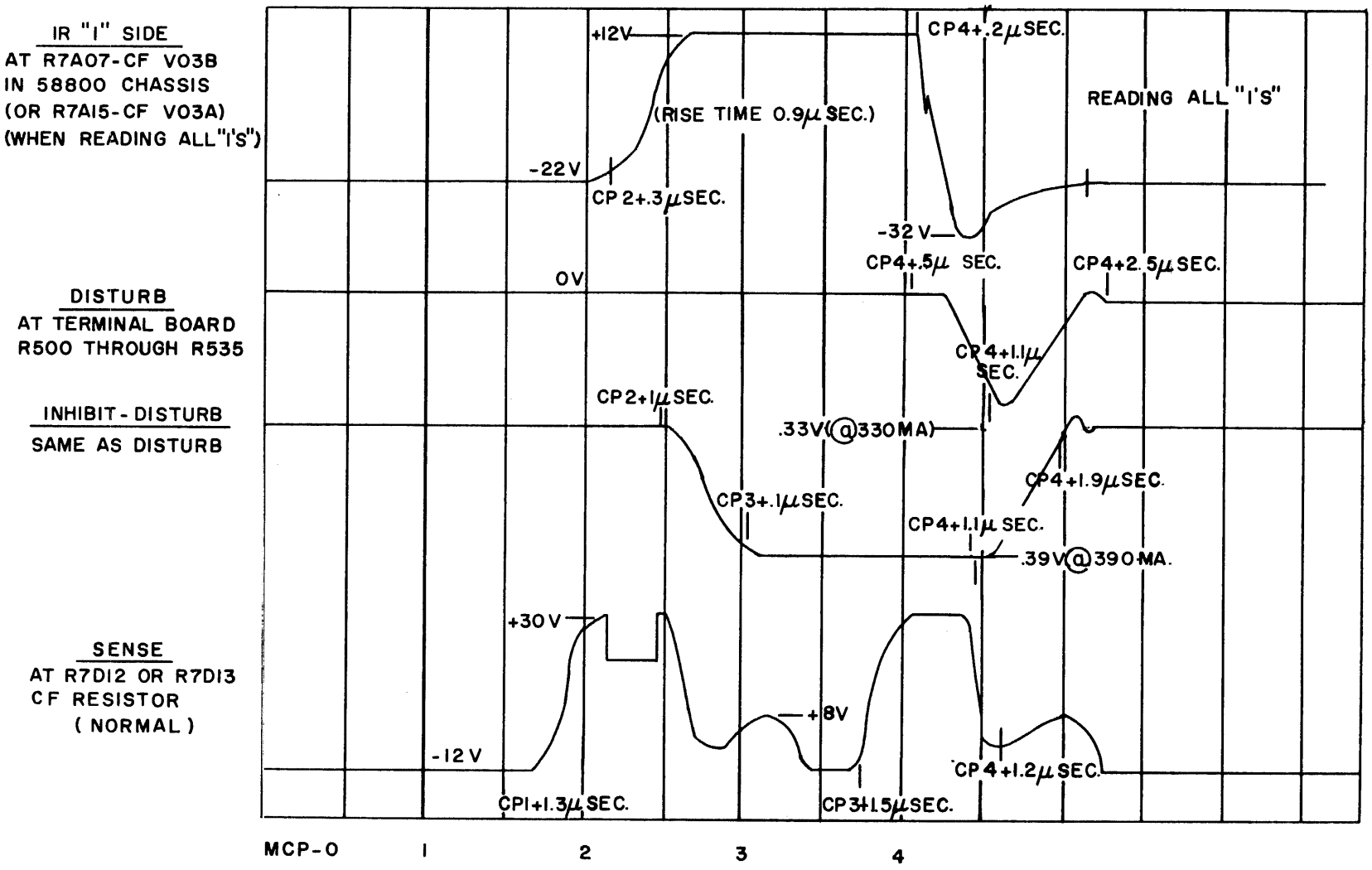

Figure 3. Typical Operating Waveforms
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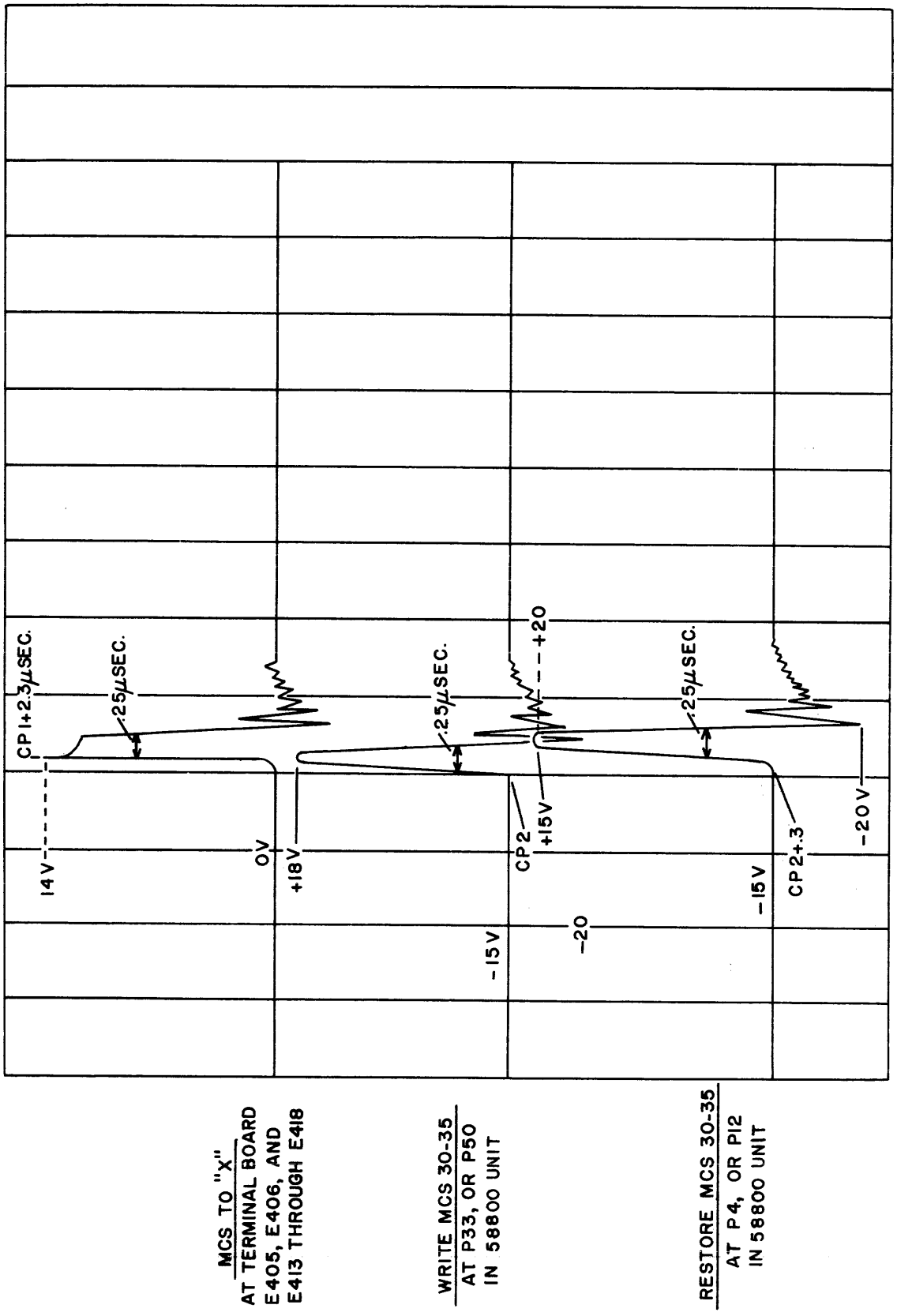

Figure 4. Typical Operating Waveforms
PX 134

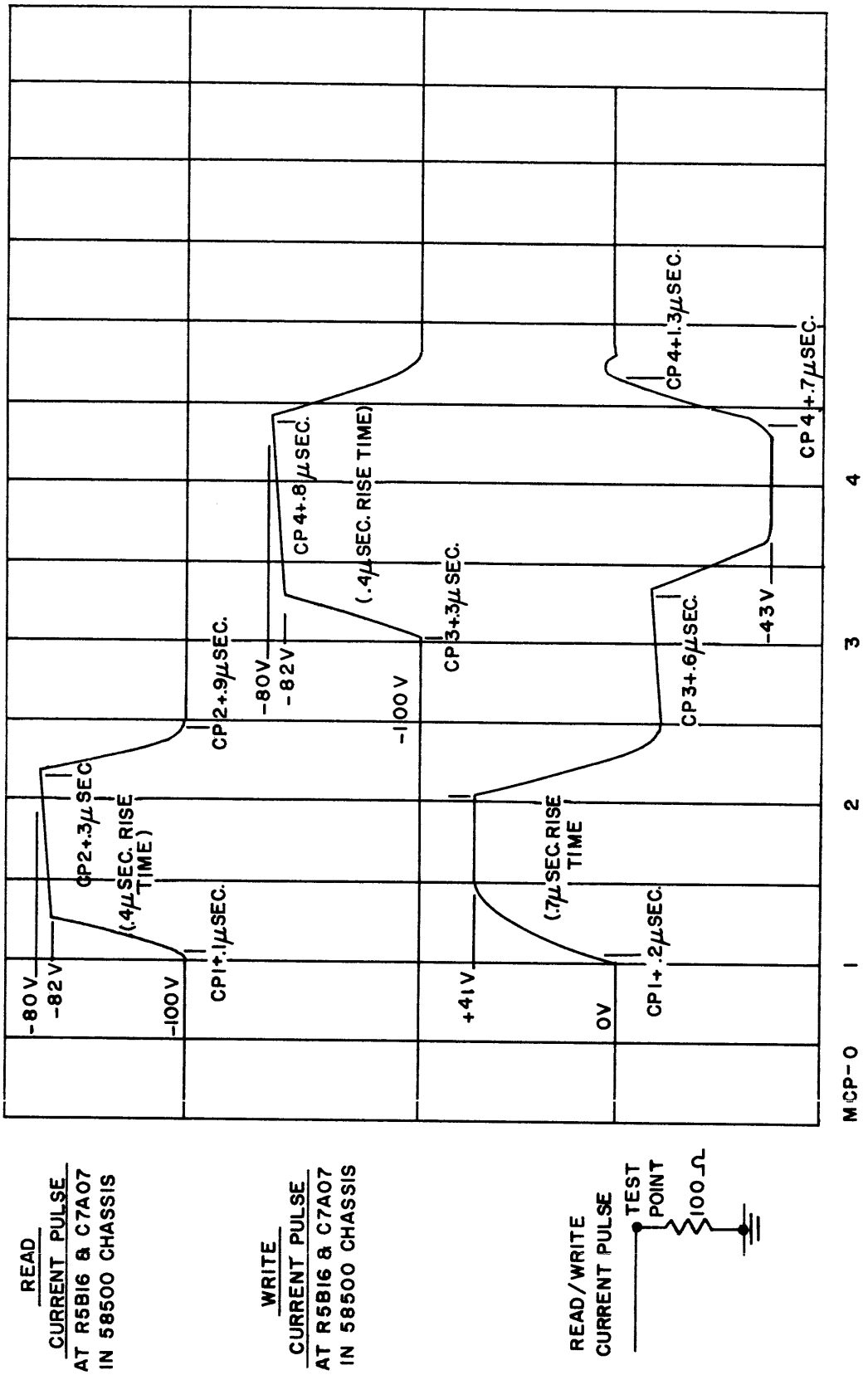

Figure 5. Typical Operating Waveforms
PX 134

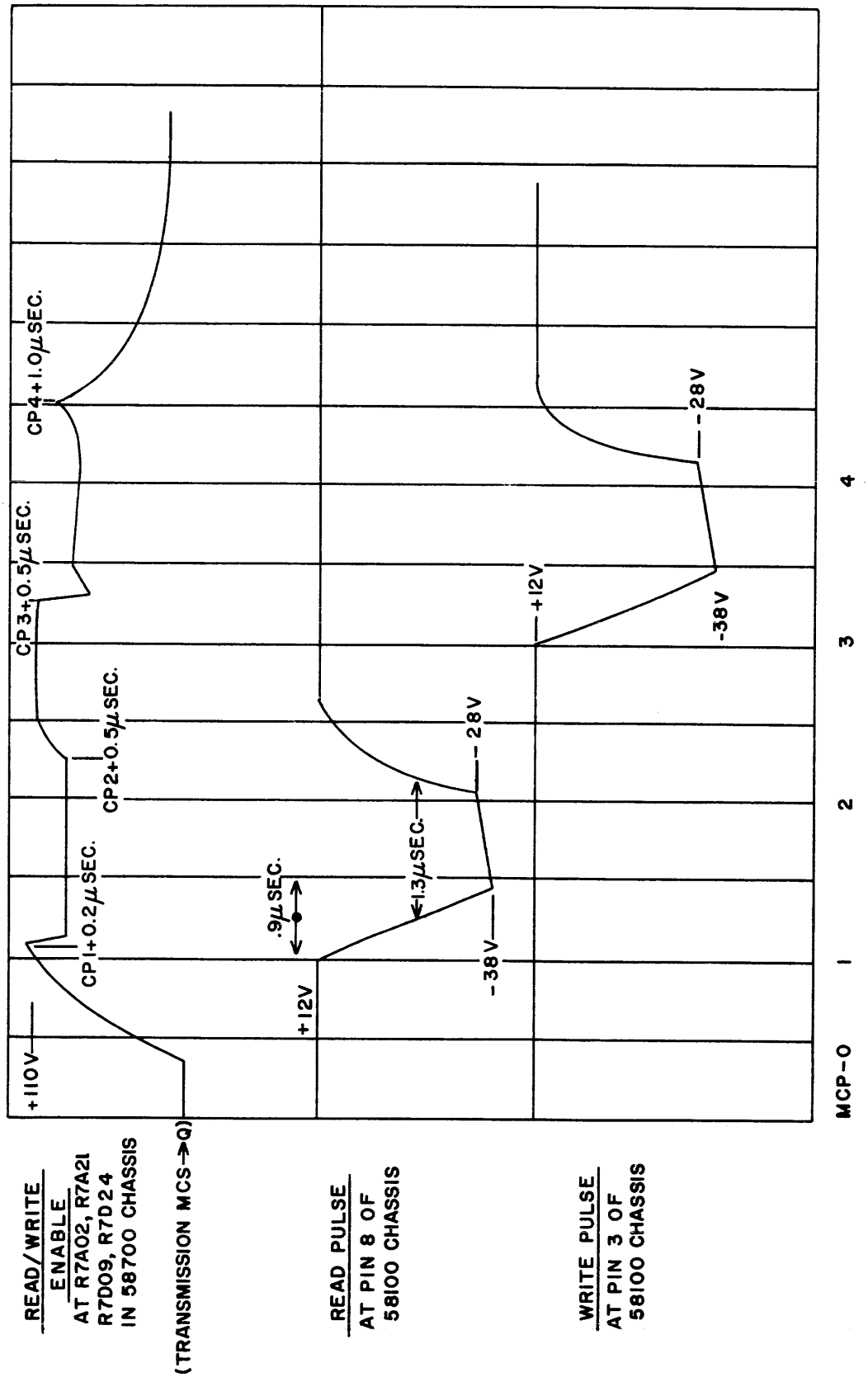

Figure 6. Typical Operating Waveforms
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TABLE 1. FUSE/INDICATOR LOCATIONS

Symbol	Location	Protects (Function)	Size (Amps)	Color of Lens
F/I 10022	10000, rear, left	Fil. transformer T10022	1	Clear
F/I 10031	↑	↑ T10031	1	↑
F/I 10032	↑	↑ T10032	1	↑
F/I 10041	↑	↑ T10041	1	↑
F/I 10042	↑	↑ T10042	1	↑
F/I 10051	↑	↑ T10051	1	↑
F/I 10052	↑	↑ T10052	1	↑
F/I 10061	↑	↑ T10061	1	↑
F/I 10062	↑	↑ T10062	1	↑
F/I 10071	↑	↑ T10071	1	↑
F/I 10072	↑	↑ T10072	1	↑
F/I 10081	↑	↑ T10081	1	↑
F/I 10082	↑	↑ T10082	1	↑
F/I 10091	↑	↑ T10091	1	↑
F/I 10092	↑	↑ T10092	1	↑
F/I 10101	↑	↑ T10101	1	↑
F/I 10102	↑	↑ T10102	1	↑
F/I 10111	↑	↑ T10111	1	↑
F/I 10112	↑	↑ T10112	1	↑
F/I 10121	↑	↑ T10121	1	↑
F/I 10122	↑	↑ T10122	1	↑
F/I 10131	↑	↑ T10131	1	↑
F/I 10132	10000, rear, left	↑ T10132	1	↑
F/I 10141	10000, rear, right	↑ T10141	1	↑
F/I 10142	↑	↑ T10142	1	↑
F/I 10151	↑	↑ T10151	1	↑
F/I 10152	↑	↑ T10152	1	↑
F/I 10161	↑	↑ T10161	1	↑
F/I 10162	↑	↑ T10162	1	↑
F/I 10171	↑	↑ T10171	1	↑
F/I 10172	↑	↑ T10172	1	↑
F/I 10181	↑	↑ T10181	1	↑
F/I 10182	↑	↑ T10182	1	↑
F/I 10191	↑	↑ T10191	1	↑
F/I 10192	↑	↑ T10192	1	↑
F/I 10201	↑	↑ T10201	1	↑
F/I 10202	↑	↑ T10202	1	↑
F/I 10211	↑	↑ T10211	1	↑
F/I 10212	↑	↑ T10212	1	↑
F/I 10221	↑	↑ T10221	1	↑
F/I 10222	↑	↑ T10222	1	↑
F/I 10231	↑	↑ T10231	1	↑
F/I 10232	↑	↑ T10232	1	↑
F/I 10241	↑	↑ T10241	1	↑
F/I 10242	↑	↑ T10242	1	↑
F/I 10251	↑	↑ T10251	1	↑
F/I 10252	10000, rear, right	Fil. transformer T10252	1	Clear

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TABLE 1. FUSE/INDICATOR LOCATIONS (Cont.)

Symbol	Location	Protects (Function)	Size (Amps)	Color of Lens
F/I 30061	30000, rear, left	Fil. transformer T30061	1	Clear
F/I 30062	↑ ↑ ↑	↑ ↑ T30062	1	↑
F/I 30071		T30071	1	
F/I 30072		T30072	1	
F/I 30081		T30081	1	
F/I 30082		T30082	1	
F/I 30091		T30091	1	
F/I 30092		T30092	1	
F/I 30101		T30101	1	
F/I 30102		T30102	1	
F/I 30111		T30111	1	
F/I 30112		T30112	1	
F/I 30121		T30121	1	
F/I 30122		T30122	1	
F/I 30131	↓ ↓ ↓	T30131	1	
F/I 30132	30000, rear, left	T30132	1	
F/I 30141	30000, rear, right	T30141	1	
F/I 30142	↑ ↑ ↑	T30142	1	
F/I 30151		T30151	1	
F/I 30152		T30152	1	
F/I 30161		T30161	1	
F/I 30162		T30162	1	
F/I 30171		T30171	1	
F/I 30172		T30172	1	
F/I 30181		T30181	1	
F/I 30182		T30182	1	
F/I 30191		T30191	1	
F/I 30192		T30192	1	
F/I 30201		T30201	1	
F/I 30202		T30202	1	
F/I 30211		T30211	1	
F/I 30212		T30212	1	
F/I 30221		T30221	1	
F/I 30222		T30222	1	
F/I 30231		T30231	1	
F/I 30232		T30232	1	
F/I 30241	↓ ↓ ↓	T30241	1	
F/I 30242	30000, rear, right	T30242	1	
		↓ ↓		
F/I 40001	40000, rear	Fil. transformer T40001	1	
F/I 42001	40000, rear	Pwr. transformer primaries	3	
F/I 55012	55000, rear	Fil. transformer T55012	1	
F/I 55021	↑ ↑	↑ ↑ T55021	1	
F/I 55022	↕ ↕	↕ ↕ T55022	1	
F/I 55031	↓ ↓	↓ ↓ T55031	1	↓
F/I 55032	55000, rear	Fil. transformer T55032	1	Clear

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TABLE 1. FUSE/INDICATOR LOCATIONS (Cont.)

Symbol	Location	Protects (Function)	Size (Amps)	Color of Lens
F/I 55041	55000, rear	Fil. transformer T55041	1	Clear
F/I 55042	↑ ↑	↑ ↑ T55042	1	↑
F/I 55051		T55051	1	
F/I 55052		T55052	1	
F/I 55062		T55062	1	
F/I 55072		T55072	1	
F/I 55082		T55082	1	
F/I 55092		T55092	1	
F/I 55101		T55101	1	
F/I 55102		T55102	1	
F/I 55111		T55111	1	
F/I 55112		T55112	1	
F/I 55121		T55121	1	
F/I 55122		T55122	1	
F/I 55131		↓ ↓ T55131	1	↓
F/I 55132		Fil. transformer T55132	1	Clear
F 55501		Magnetic Core Matrix	1/2	None
thru	↓ ↓	drive lines		↕
F 55663	55000, rear			None
F/I 60021	60000, rear, left	Fil. transformer T60021	1	Clear
F/I 60022	↑ ↑ ↑	↑ ↑ T60022	1	↑
F/I 60031		T60031	1	
F/I 60032		T60032	1	
F/I 60041		T60041	1	
F/I 60042		T60042	1	
F/I 60051		T60051	1	
F/I 60052		T60052	1	
F/I 60061		T60061	1	
F/I 60062		T60062	1	
F/I 60071		T60071	1	
F/I 60072		T60072	1	
F/I 60081		T60081	1	
F/I 60082		T60082	1	
F/I 60091		T60091	1	
F/I 60092		T60092	1	
F/I 60101		T60101	1	
F/I 60102		T60102	1	
F/I 60111		T60111	1	
F/I 60112		T60112	1	
F/I 60121		T60121	1	
F/I 60122		T60122	1	
F/I 60131	↓ ↓ ↓	T60131	1	
F/I 60132	60000, rear, left	T60132	1	
F/I 60141	60000, rear, right	T60141	1	
F/I 60142	↕ ↕ ↕	↓ ↓ T60142	1	↓
F/I 60151	60000, rear, right	Fil. transformer T60151	1	Clear

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TABLE 1. FUSE/INDICATOR LOCATIONS (Cont.)

Symbol	Location	Protects (Function)	Size (Amps)	Color of Lens
F/I 60152	60000, rear, right	Fil. transformer T60152	1	Clear
F/I 60161	↑ ↑ ↑	T60161	1	↑
F/I 60162		T60162	1	
F/I 60171		T60171	1	
F/I 60172	60000, rear, right	T60172	1	
F/I 70041	70000, rear, left	T70041	1	
F/I 70042	↑ ↑ ↑	T70042	1	
F/I 70051		T70051	1	
F/I 70052		T70052	1	
F/I 70061		T70061	1	
F/I 70062		T70062	1	
F/I 70071		T70071	1	
F/I 70072		T70072	1	
F/I 70081		T70081	1	
F/I 70082		T70082	1	
F/I 70091		T70091	1	
F/I 70092		T70092	1	
F/I 70101		T70101	1	
F/I 70102		T70102	1	
F/I 70111		T70111	1	
F/I 70112		T70112	1	
F/I 70121		T70121	1	
F/I 70122		T70122	1	
F/I 70131	↓ ↓ ↓	T70131	1	
F/I 70132	70000, rear, left	T70132	1	
F/I 70141	70000, rear, right	T70141	1	
F/I 70142	↑ ↑ ↑	T70142	1	
F/I 70151		T70151	1	
F/I 70152		T70152	1	
F/I 70161		T70161	1	
F/I 70162		T70162	1	
F/I 70171		T70171	1	
F/I 70172		T70172	1	
F/I 70181		T70181	1	
F/I 70182		T70182	1	
F/I 70191		T70191	1	
F/I 70192		T70192	1	
F/I 70201		T70201	1	
F/I 70202		T70202	1	
F/I 70211		T70211	1	
F/I 70212		T70212	1	
F/I 70221		T70221	1	
F/I 70222		T70222	1	
F/I 70231		T70231	1	
F/I 70232	↓ ↓ ↓	T70232	1	↓
F/I 70241	70000, rear, right	Fil. transformer T70241	1	Clear

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TABLE 1. FUSE/INDICATOR LOCATIONS (Cont.)

Symbol	Location	Protects (Function		Size (Amps)	Color of Lens
F/I 70242	70000, rear, right	Fil. transformer	T70242	1	Clear
F/I 70251	↕ ↕ ↕	↑ ↑	T70251	1	↑
F/I 70252	70000, rear, right	↓ ↓	T70252	1	
F/I 81401	80000, front, right	Fil. transformer	T81401	1	
F/I 81601	80000, rear, left	Arithmetic	+200 vdc	3	
F/I 81602	↑ ↑ ↑	↑	+150 vdc	4	
F/I 81603		↓	+100 vdc	2	
F/I 81604		Arithmetic	+ 80 vdc	1	
F/I 81605		Output	+ 5 vdc	1	
F/I 81606		Output	- 15 vdc	1	
F/I 81607		Arithmetic	- 80 vdc	5	
F/I 81608		Arithmetic	+ 60 vdc	1	
F/I 81609		Control	+200 vdc	2	
F/I 81610		↑	+150 vdc	5	
F/I 81611			+100 vdc	1/2	
F/I 81612			+ 80 vdc	1/2	
F/I 81613			- 80 vdc	5	
F/I 81614			- 30 vdc	1/2	
F/I 81615		↓	+ 60 vdc	1	
F/I 81616		Control	+120 vdc(relay)	1	
F/I 81617		Mag. drum	+200 vdc	1	
F/I 81618		↑ ↑	+150 vdc	5	
F/I 81619			+100 vdc	2	
F/I 81620			+ 80 vdc	1/2	
F/I 81621		↓ ↓	- 80 vdc	4	
F/I 81622		Mag. drum	- 25 vdc	1/2	
F/I 81623		Ext. equip.	+200 vdc	1	
F/I 81624		↑ ↑	+150 vdc	1	
F/I 81625			+100 vdc	1	
F/I 81626			+ 80 vdc	1	
F/I 81627			+ 5 vdc	1/2	
F/I 81628			- 15 vdc	1/2	
F/I 81629			- 80 vdc	1/2	
F/I 81630			+ 60 vdc	1	
F/I 81631		↓ ↓	+120 vdc(relay)	1	
F/I 81632		Ext. equip.	110 vac	5	
F/I 81635		Mag. core	+200 vdc	10	
F/I 81636		↑ ↑	+150 vdc	5	
F/I 81637			+100 vdc	2	
F/I 81638			+ 80 vdc	1	
F/I 81639			- 80 vdc	5	
F/I 81640			-100 vdc	3	
F/I 81641			-200 vdc	2	
F/I 81642		Mag. core	- 35 vdc	1	
F/I 81643	↓ ↓ ↓	Mag. tape	+270 vdc	3	↓
F/I 81644	80000, rear, left	Mag. tape	+200 vdc	2	Clear

TABLE 1. FUSE/INDICATOR LOCATIONS (Cont.)

Symbol	Location	Protects (Function)	Size (Amps)	Color of Lens
F/I 81645	80000, rear, left	Mag. tape +150 vdc	4	Clear
F/I 81646	↑ ↑ ↑	↑ ↑ +120 vdc	2	↑
F/I 81647	↕ ↕ ↕	↕ ↕ +100 vdc	1/2	↕
F/I 81648	↕ ↕ ↕	↕ ↕ + 80 vdc	1	↕
F/I 81649	↕ ↕ ↕	↕ ↕ - 80 vdc	4	↕
F/I 81650	↕ ↕ ↕	↕ ↕ -150 vdc	2	↕
F/I 81651	↓ ↓ ↓	↓ ↓ -300 vdc	1	↕
F/I 81652	80000, rear, left	Mag. tape + 60 vdc	2	↕
F/I 81701	80000, rear, right	Pwr. transformers primaries	1/4	↕
F/I 81702	↑ ↑ ↑	81700 voltage rectifier	1/2	↕
F/I 81703	↕ ↕ ↕	circuits.	1/2	↕
F/I 81704	↕ ↕ ↕	Output - 30 vdc	1/2	↕
F/I 81705	↕ ↕ ↕	Output +120 vdc	1/2	↕
F/I 81706	80000, rear, right	Output + 60 vdc	2	↕
F/I 83001	80000, front, (+200V)	+200 V mag amp, a-c input	20	↕
F/I 83002	↑ ↑ ↑	↑ ↑ ↑ a-c input	20	↕
F/I 83003	↕ ↕ ↕	↕ ↕ ↕ a-c input	20	↕
F/I 83004	↕ ↕ ↕	↕ ↕ ↕ ref input	1	Clear
F/I 83005	(+200V)	+200 V mag amp, d-c output	20	Amber
F/I 83101	(-150V)	-150 V mag amp, a-c input	3	Clear
F/I 83102	↑ ↑ ↑	↑ ↑ ↑ a-c input	3	↑
F/I 83103	↕ ↕ ↕	↕ ↕ ↕ a-c input	3	↕
F/I 83104	↕ ↕ ↕	↕ ↕ ↕ ref input	1	Clear
F/I 83105	(-150V)	-150 V mag amp, d-c output	4	Amber
F/I 83201	(+120V)	+120 V mag amp, a-c input	3	Clear
F/I 83202	↑ ↑ ↑	↑ ↑ ↑ a-c input	3	↑
F/I 83203	↕ ↕ ↕	↕ ↕ ↕ a-c input	3	↕
F/I 83204	↕ ↕ ↕	↕ ↕ ↕ ref input	1	Clear
F/I 83205	(+120V)	+120 V mag amp, d-c output	4	Amber
F/I 83301	(+100V)	+100 V mag amp, a-c input	3	Clear
F/I 83302	↑ ↑ ↑	↑ ↑ ↑ a-c input	3	↑
F/I 83303	↕ ↕ ↕	↕ ↕ ↕ a-c input	3	↕
F/I 83304	↕ ↕ ↕	↕ ↕ ↕ ref input	1	Clear
F/I 83305	(+100V)	+100 V mag amp, d-c output	6	Amber
F/I 83401	(+80V)	+80 V mag amp, a-c input	3	Clear
F/I 83402	↑ ↑ ↑	↑ ↑ ↑ a-c input	3	↑
F/I 83403	↕ ↕ ↕	↕ ↕ ↕ a-c input	3	↕
F/I 83404	↕ ↕ ↕	↕ ↕ ↕ ref input	1	Clear
F/I 83405	(+80V)	+80 V mag amp, d-c output	6	Amber
F/I 83501	(-35V)	-35 V mag amp, a-c input	1/2	Clear
F/I 83502	↑ ↑ ↑	↑ ↑ ↑ a-c input	1/2	↑
F/I 83503	↕ ↕ ↕	↕ ↕ ↕ a-c input	1/2	↕
F/I 83504	↕ ↕ ↕	↕ ↕ ↕ ref input	1	Clear
F/I 83505	(-35V)	-35 V mag amp, d-c output	1	Amber
F/I 83601	(-15V)	-15 V mag amp, a-c input	1/2	Clear
F/I 83602	↕ ↕ ↕	↕ ↕ ↕ a-c input	1/2	↕
F/I 83603	80000, front (-15V)	-15 V mag amp, a-c input	1/2	Clear

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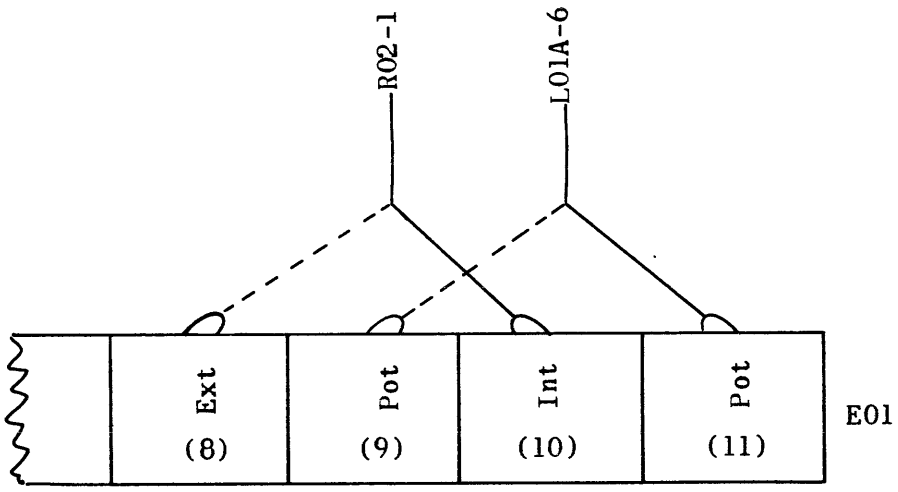
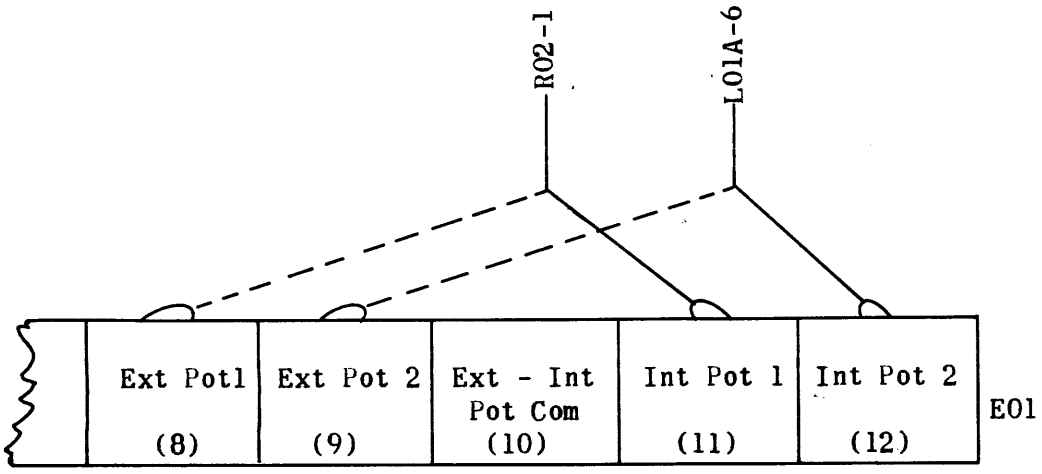
TABLE 1. FUSE/INDICATOR LOCATIONS (Cont.)

Symbol	Location	Protects (Function)	Size (Amps)	Color of Lens
F/I 83604	80000, front (-15V)	-15 V mag amp,ref input	1	Clear
F/I 83605	↑ ↑ (-15V)	-15 V mag amp,d-c output	2	Amber
F/I 83701	↑ ↑ (+5V)	+5 V mag amp,a-c input	1/2	Clear
F/I 83702	↑ ↑ ↑	↑ ↑ ↑ a-c input	1/2	↑
F/I 83703	↕ ↕ ↕	↕ ↕ ↕ a-c input	1/2	↓
F/I 83704	↓ ↓ ↓	↓ ↓ ↓ ref input	1	Clear
F/I 83705	↑ ↑ (+5V)	+5 V mag amp,d-c output	2	Amber
F/I 83801	↑ ↑ (+150V)	+150 V mag amp,a-c input	20	Clear
F/I 83802	↑ ↑ ↑	↑ ↑ ↑ a-c input	20	↑
F/I 83803	↕ ↕ ↕	↕ ↕ ↕ a-c input	20	↓
F/I 83804	↓ ↓ ↓	↓ ↓ ↓ ref input	1	Clear
F/I 83805	↑ ↑ (+150V)	+150 V mag amp,d-c output	30	Amber
F/I 83901	↑ ↑ (-80V)	-80 V mag amp,a-c input	12	Clear
F/I 83902	↑ ↑ ↑	↑ ↑ ↑ a-c input	12	↑
F/I 83903	↕ ↕ ↕	↕ ↕ ↕ a-c input	12	↓
F/I 83904	↓ ↓ ↓	↓ ↓ ↓ ref input	1	Clear
F/I 83905	↑ ↑ (-80V)	-80 V mag amp,d-c output	30	Amber
F/I 84001	↑ ↑ (-300V)	-300 V mag amp,a-c input	5	Clear
F/I 84002	↑ ↑ ↑	↑ ↑ ↑ a-c input	5	↑
F/I 84003	↕ ↕ ↕	↕ ↕ ↕ a-c input	5	↓
F/I 84004	↓ ↓ ↓	↓ ↓ ↓ ref input	1	Clear
F/I 84005	↑ ↑ (-300V)	-300 V mag amp,d-c output	4	Amber
F/I 84101	↑ ↑ (+270V)	+270 V mag amp,a-c input	5	Clear
F/I 84102	↑ ↑ ↑	↑ ↑ ↑ a-c input	5	↑
F/I 84103	↕ ↕ ↕	↕ ↕ ↕ a-c input	5	↓
F/I 84104	↓ ↓ ↓	↓ ↓ ↓ ref input	1	Clear
F/I 84105	↑ ↑ (+270V)	+270 V mag amp,d-c output	4	Amber
F/I 84201	↑ ↑ (-200V)	-200 V mag amp,a-c input	3	Clear
F/I 84202	↑ ↑ ↑	↑ ↑ ↑ a-c input	3	↑
F/I 84203	↕ ↕ ↕	↕ ↕ ↕ a-c input	3	↓
F/I 84204	↓ ↓ ↓	↓ ↓ ↓ ref input	1	Clear
F/I 84205	↑ ↑ (-200V)	-200 V mag amp,d-c output	3	Amber
F/I 84301	↑ ↑ (-100V)	-100 V mag amp,a-c input	3	Clear
F/I 84302	↑ ↑ ↑	↑ ↑ ↑ a-c input	3	↑
F/I 84303	↕ ↕ ↕	↕ ↕ ↕ a-c input	3	↓
F/I 84304	↓ ↓ ↓	↓ ↓ ↓ ref input	1	Clear
F/I 84305	80000, front (-100V)	-100 V mag amp,d-c output	6	Amber



POWER SUPPLIES PS1A-1, PS1A-2, PS2A-1, PS2A-2, PS5A-2, PS5A-3, PS6A-1, PS1B-1, PS2B-1 AND PS3B-1.



POWER SUPPLY PS13A-1

Figure 7. Connections for Internal and External Pots
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Step 4. Before applying power, make a visual check of power supply components and wire connections.

(2) SYSTEM TROUBLE SHOOTING. - Table 2 describes procedures necessary to determine which element of the unit is at fault, the probable cause, and remedy.

Table 3 shows typical voltage and resistance measurements of circuits for each power supply with points of measurement. Resistance measurements were taken with a Simpson Model 260 VOM; voltage measurements with a Triplett Model 630 AVOM; RMS voltages were measured with "output" ranges to show a-c voltage components between points of measurement.

Voltage and resistance measurements were taken on one power supply of each type. However, values should be approximately the same on all supplies of each type. Measurements on the current reference supplies may vary slightly on different units. Measurements of voltage in reactor, magnetic amplifier rectifier, and transformer circuits may vary over a larger or smaller range than those indicated on the charts, depending upon the electrical balance of the three power supply phases and the associated phase impedances within the power supply.

b. RELAY PANELS, SWITCH PANELS, AND SENSING CIRCUITS. - The remaining units of the power supply system are, in general, relatively simple, and malfunctioning components are easily detected and corrected. The Power Sequencing Circuit, 81200, the Power Control Panel, 81800, and the Power Sequence Control, 81900, are essentially relay chassis. The Voltage Senser, 81400, contains relay puller circuits. The D-C Distribution Panel mounts the distribution control switches and d-c overload fuses, while the Circuit Breaker Panel contains the overload breakers.

NOTE

RELAY CONTACTS SHOULD NEVER BE DRESSED; IF A RELAY DOES NOT OPERATE EFFICIENTLY, REPLACE THE RELAY.

TABLE 2

TROUBLE-SHOOTING CHART

SYMPTOM	PROBABLE CAUSE	REMEDY
1. No output voltage	1. Accidental overload of power supply.	1. Check B+ and line fuses. If open, check load circuit before replacing fuses.
2. Unit blows line fuse, or fuses, when input power applied.	1. Failure of one or more output rectifiers because of repeated accidental overloads.	1. Check forward and reverse resistance of output rectifiers (CR1 thru CR6) according to resistance charts. Replace if defective.
3. Unit blows B+ fuse when input power applied.	1. Insufficient lapse of time for time delay relay element cooling.	1. Allow unit to remain off at least 30 seconds before reapplying power.
	2. Time delay relay contacts fail to open with power removed.	1. Check continuity of time delay relay contacts. If contacts remain closed with power removed, replace relay.
4. Unit blows B+ fuse after time delay relay closes.	1. Breakdown of filter capacitor, C01, or rate capacitor, C02.	1. Remove either or both capacitors, C01 and C02, from the circuit. Apply power to the unit, determine which capacitor is faulty. Replace faulty capacitor. (Note: After a long period of storage, the insulating oxide film in this type of capacitor may become degenerated. With this condition, attempt to restore the capacitor by applying nominal capacitor voltage, d-c, thru a resistor of 100 ohms for 5 to 10 minutes).
5. Unit blows current reference line fuses.	1. Failure of current reference unit.	1. Check current reference resistance measurements according to voltage and resistance charts. Replace current reference unit if faulty.

TABLE 2. TROUBLE-SHOOTING CHART (Cont.)

SYMPTOM	PROBABLE CAUSE	REMEDY
	2. Breakdown of current reference filter capacitor, C03.	1. Apply power to unit with capacitor C03 removed from the circuit or with substitute capacitor. Replace defective capacitor.
6. Output voltage lower than normal but can be varied by potentiometer control.	1. Open reactor power windings.	1. Check continuity of reactor power windings (1 to 2). If open, replace reactor pair.
	2. Open power transformer windings.	1. Check continuity of transformer primary and secondary windings. Replace transformer if windings are open.
7. Output voltage lower than normal and no control of voltage.	1. Failure of current reference unit or associated circuits.	1. Check output voltage of current reference unit; make resistance checks. Replace faulty unit.
		2. Check continuity of resistors R01 and R02. Replace if defective.
		3. Check continuity of reactor reference windings (5 to 6). Replace reactor pair if winding is open or shorted.
8. Output voltage higher than normal; no voltage regulation.	1. Open control winding circuit.	1. Check resistance of R03. Replace if defective.
		2. Check continuity of reactor control winding (3 to 4). If open or shorted, replace reactor pair.
9. Poor steady state voltage regulation.	1. Defective mag. amp. rectifiers.	1. Check mag. amp. rectifier (CR07 thru CR12) forward and reverse resistance according to resistance chart. Replace rectifiers if defective.

TABLE 2. TROUBLE-SHOOTING CHART (Cont.)

SYMPTOM	PROBABLE CAUSE	REMEDY
10. Poor voltage regulation under transient conditions.	1. Open rate circuit.	1. Determine if rate capacitor, C02, is faulty. Replace if faulty.
		2. Check continuity of reactor rate winding, (7 to 8). If open or shorted, replace reactor pair.
	2. Defective mag. amp. rectifiers.	1. Check forward and reverse resistance of mag. amp. rectifiers (CR07 thru CR12) according to resistance chart. Replace defective rectifier or rectifiers.
11. Large amount of ripple in output voltage.	1. Time delay relay contacts not closing.	1. After sufficient time to close time delay relay (20 seconds), ascertain if charging resistor, R05, is shorted. If R05 is not shorted, check shorting circuit. Replace relay if defective.
		2. Check continuity of time delay relay heating element. If open, replace relay.
	2. Open circuit in filter capacitor, C01.	1. Check filter capacitor, C01. Replace capacitor if defective.
12. Ripple in output voltage is slightly greater than normal.	1. Defective mag. amp. rectifiers.	1. Measure mag. amp. rectifier (CR07 thru CR12) forward and reverse resistance. Replace defective rectifiers.
	2. Shorted turn in reactor power winding.	1. Check voltage and resistance measurements on reactor power windings (1 to 2). Replace reactor pair if found defective.
	3. Defective filter capacitor, C01.	1. Substitute new capacitors and note any change in ripple. Replace defective capacitors.

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS6A-1 (+270 Volt Unit)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:	RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp., CR07-CR12	0 to 2	0 to 1	1.5	6.0
Output, CR01-CR06	150	-150	1.6	1500
Stabilizing, CR13	-	-	-	-

RESISTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Voltage Cont., R01	-	17	(+ lead on R01-1) 170
Bias Setting, R02	-	17	(+ lead on R02-3) 85
Cont. Winding, R03	0.1	270	(+ lead on R03-3) 1200
Current Ref. Pri., R04	47	-	100
Capacitor Charging, R05	Shorted out by relay after 20 seconds		
Stabilizing, R07	-	-	(+ lead on R07-3) -

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	170	0.8
Primary 1 to 3	164	0.8
Primary 2 to 3	157	0.8
Secondary A to Neutral	138	1.0
Secondary B to Neutral	141	1.0
Secondary C to Neutral	135	1.0

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
1 to 2	10 to 60	-	2.2
3 to 4	10 to 75	5.4	26
5 to 6	10 to 75	5.4	26
7 to 8	3 to 20	-	0.65
L01A-3 to L03B-3	0	32	(+ lead on L01A-3) 156
L01A-6 to L03B-6	3.0	32	(+ lead on L01A-6) 156
L01A-7 to L03B-7	-	-	(+ lead on L01A-7) 3.9

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Line input, E04 to E05	111	-	100
Pin 1 to Pin 3	70	-	5
Pin 5 to Pin 7	3.5	65	(+ lead on 5) 400

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS1A-1 (+200 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:		RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp.,	CR07-CR12	0 to 0.7	0 to 0.4	2.5	3.2
Output,	CR01-CR06	59 to 69	-91 to 111	2.2	1500 to 1760
Stabilizing,	CR13	-	-	-	-

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	17	(+ lead on R01-1)	350
Bias Setting,	R02	-	7.3	(+ lead on R02-3)	43
Cont. Winding,	R03	1.0	161	(+ lead on R03-3)	600
Current Ref. Pri.,	R04	27	-		100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds			
Stabilizing,	R07	-	-	(+ lead on R07-3)	-

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	105	0.1
Primary 1 to 3	102	0.1
Primary 2 to 3	114	0.1
Secondary A to Neutral	52	0.05
Secondary B to Neutral	57	0.05
Secondary C to Neutral	60	0.05

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	54 to 55	-	0.3	
3 to 4	144 to 150	7.2	37	
5 to 6	140 to 151	6.0	37	
7 to 8	41 to 43	-	1.0	
L01A-3 to L03B-3	1.0	43.2	(+ lead on L01A-3)	300
L01A-6 to L03B-6	1.5	37	(+ lead on L01A-6)	210
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	5.9

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	88	-	105	
Pin 1 to Pin 3	63	-	5.8	
Pin 5 to Pin 7	2.15	60	(+ lead on 5)	580

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS1B-1 (+150 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no lead. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:	RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp., CR07-CR12	0.65 to 1.1	0 to 0.3	10	11
Output, CR01-CR06	55 to 60	-57 to 95	9.0	1500
Stabilizing, CR13	-	-	-	-

RESISTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont., R01	-	29	(+ lead on R01-1)	340
Bias Setting, R02	-	0.9	(+ lead on R02-3)	4.0
Cont. Winding, R03	1.05	121	(+ lead on R03-3)	550
Current Ref. Pri., R04	29	-		100
Capacitor Charging, R05	Shorted out by relay after 20 seconds			
Stabilizing, R07	-	-	(+ lead on R07-3)	-

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	108	0.1
Primary 1 to 3	120	0.1
Primary 2 to 3	118	0.1
Secondary A to Neutral	44	0.05
Secondary B to Neutral	49	0.05
Secondary C to Neutral	50	0.05

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	40 to 57	-	0.3	
3 to 4	110 to 155	4.7	25	
5 to 6	110 to 155	4.5	25	
7 to 8	31 to 44	-	1.0	
L01A-3 to L03B-3	1.05	32.7	(+ lead on L01A-3)	175
L01A-6 to L03B-6	1.4	30	(+ lead on L01A-6)	175
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	5.8

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	92	-	100	
Pin 1 to Pin 3	64	-	5.0	
Pin 5 to Pin 7	2.2	59	(+ lead on 5)	500

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS2A-1 (+120 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:		RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp.,	CR07-CR12	0.4 to 0.9	0.15 to 0.55	3.3	12.8
Output,	CR01-CR06	53 to 56	-58	2.5	370
Stabilizing,	CR13	-	-	-	-

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	12.9	(+ lead on R01-1)	220
Bias Setting,	R02	-	17.3	(+ lead on R02-3)	90
Cont. Winding,	R03	0.65	92	(+ lead on R03-3)	410
Current Ref. Pri.,	R04	27.2	-		100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds			
Stabilizing,	R07	-	-	(+ lead on R07-3)	-

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	162	1.7
Primary 1 to 3	155	1.7
Primary 2 to 3	158	1.7
Secondary A to Neutral	49.8	.25
Secondary B to Neutral	51	.25
Secondary C to Neutral	48	.25

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	31 to 43	-	3.7	
3 to 4	36.5 to 50	4.8	24	
5 to 6	36.5 to 50	4.8	24.5	
7 to 8	10 to 12	-	0.6	
L01A-3 to L03B-3	0.65	28.8	(+ lead on L01A-3)	150
L01A-6 to L03B-6	1.16	28.7	(+ lead on L01A-6)	150
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	3.8

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Line input, E04 to E05	90	-	105
Pin 1 to Pin 3	62	-	5.2
Pin 5 to Pin 7	1.9	58	(+ lead on 5) 560

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS2A-2 (+100 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:	RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp., CR07-CR12	0 to 1.6	0 to 1.2	3.6	13.2
Output, CR01-CR06	30 to 42	-35	2.6	240
Stabilizing, CR13	-	-	2.9	570

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	17	(+ lead on R01-1)	350
Bias Setting,	R02	-	17	(+ lead on R02-3)	90
Cont. Winding,	R03	4.0	72	(+ lead on R03-3)	340
Current Ref. Pri.,	R04	32	-		100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds			
Stabilizing,	R07	-	-	(+ lead on R07-3)	190

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	135	1.8
Primary 1 to 3	120	1.8
Primary 2 to 3	125	1.8
Secondary A to Neutral	38.2	0.175
Secondary B to Neutral	35.3	0.175
Secondary C to Neutral	34.2	0.175

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	35 to 70	-	4.2	
3 to 4	40 to 80	5.0	24	
5 to 6	40 to 80	4.6	24	
7 to 8	11 to 20	-	0.65	
L01A-3 to L03B-3	4.0	30	(+ lead on L01A-3)	150
L01A-6 to L03B-6	3.9	27	(+ lead on L01A-6)	150
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	4.2

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	94	-	105	
Pin 1 to Pin 3	64	-	5.7	
Pin 5 to Pin 7	3.4	60	(+ lead on 5)	580

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS2A-2 (+80 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:		RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp.,	CR07-CR12	0 to 1	0 to 1	3.6	13.0
Output,	CR01-CR06	37	-37	2.6	220
Stabilizing,	CR13	-	-	-	-

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	11	(+ lead on R01-1)	350
Bias Setting,	R02	-	17	(+ lead on R02-3)	85
Cont. Winding,	R03	0	50	(+ lead on R03-3)	240
Current Ref. Pri.,	R04	32	-		100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds			
Stabilizing,	R07	-	-	(+ lead on R07-3)	180

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	158	1.8
Primary 1 to 3	154	1.8
Primary 2 to 3	156	1.8
Secondary A to Neutral	33	0.12
Secondary B to Neutral	34.2	0.12
Secondary C to Neutral	32.4	0.12

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	30 to 50	-	4	
3 to 4	30 to 60	5.0	24	
5 to 6	30 to 60	5.0	24	
7 to 8	9 to 15	-	0.65	
L01A-3 to L03B-3	0	30	(+ lead on L01A-3)	150
L01A-6 to L03B-6	1.2	29	(+ lead on L01A-6)	150
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	4.0

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	94	-	105	
Pin 1 to Pin 3	62	-	5.7	
Pin 5 to Pin 7	2.0	57	(+ lead on 5)	580

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS13A-1 (+5V)(3 to 8 Volt Unit)(Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:	RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp., CR07-CR12	0.7 to 1.05	0.4 to 0.8	3.9	150
Output, CR01-CR06	1.7 to 1.9	-2.40	3.3	33
Stabilizing, DR13	-	0.35	3.4	39

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	29.2	(+ lead on R01-1)	340
Bias Setting,	R02	-	26.7	(+ lead on R02-3)	140
Cont. Winding,	R03	0	0	(+ lead on R03-3)	0
Current Ref. Pri.,	R04	41.0	-		100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds			
Stabilizing,	R07	-	4.8	(+ lead on R07-3)	24

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	80	34
Primary 1 to 3	74	34
Primary 2 to 3	80	38
Secondary A to Neutral	1.8	0.15
Secondary B to Neutral	1.75	0.15
Secondary C to Neutral	1.63	0.15

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	75 to 80	-	62	
3 to 4	15.2 to 16.0	0.75	4.5	
5 to 6	15.2 to 16.0	0.75	4.8	
7 to 8	3.0 to 3.1	-	0.3	
L01A-3 to L03B-3	0	4.5	(+ lead on L01A-3)	21
L01A-6 to L03B-6	0.2	4.5	(+ lead on L01A-6)	17
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	1.5

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	105	-	105	
Pin 1 to Pin 3	65	-	5.9	
Pin 5 to Pin 7	2.55	58.8	(+ lead on 5)	480

ADDITIONAL COMPONENTS	D.C. VOLTAGE	RESISTANCE
Voltage Range Adjust, R8	0.80 Volts	17 Ohms
Bleeder Resistor, R10	5.0	21
Filter Choke, L4	---	0.1

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TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS5A-3 (-15 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:	RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp., CR07-CR12	0.7 to 1.2	0.55 to 0.85	4.0	150
Output, CR01-CR06	4.6 to 5.2	-6.2	3.3	80
Stabilizing, CR13	-	-	-	-

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	25.5	(+ lead on R01-1)	330
Bias Setting,	R02	-	27.0	(+ lead on R02-3)	130
Cont. Winding,	R03	0.05	9.7	(+ lead on R03-3)	40
Current Ref. Pri.,	R04	41.5	-		100
Capacitor Charging,	R05	Shorted out by relay after		20 seconds	
Stabilizing,	R07	-	-	(+ lead on R07-3)	-

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	118	17
Primary 1 to 3	94	17
Primary 2 to 3	128	19
Secondary A to Neutral	5.5	0.2
Secondary B to Neutral	5.8	0.2
Secondary C to Neutral	4.3	0.2

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	30 to 80	-	62	
3 to 4	6.0 to 16.5	0.85	4.5	
5 to 6	6.0 to 16.5	0.85	4.8	
7 to 8	1.7 to 4.7	-	0.35	
L01A-3 to L03B-3	0.05	5.0	(+ lead on L01A-3)	23
L01A-6 to L03B-6	0.25	5.1	(+ lead on L01A-6)	27
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	1.5

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	106	-	100	
Pin 1 to Pin 3	63	-	6.0	
Pin 5 to Pin 7	2.3	57.5	(+ lead on 5)	480

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS5A-2 (-35 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:	RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp., CR07-CR12	1.8 to 2.7	0.8 to 1.4	3.8	145
Output, CR01-CR06	13.9 to 15.5	-15.8 to 17.5	3.5	245
Stabilizing, CR13	-	-	-	-

RESISTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Voltage Cont., R01	-	21.8	(+ lead on R01-1) 350
Bias Setting, R02	-	29.7	(+ lead on R02-3) 140
Cont. Winding, R03	0.15	29.5	(+ lead on R03-3) 130
Current Ref. Pri., R04	29.7	-	100
Capacitor Charging, R05	Shorted out by relay after 20 seconds		
Stabilizing, R07	-	-	(+ lead on R07-3) -

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	152	16.5
Primary 1 to 3	126	16.5
Primary 2 to 3	159	18.5
Secondary A to Neutral	14.8	0.6
Secondary B to Neutral	15.2	0.6
Secondary C to Neutral	12.0	0.6

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
1 to 2	22 to 73	-	60
3 to 4	5.0 to 14.7	0.9	4.4
5 to 6	5.0 to 14.7	0.9	4.7
7 to 8	1.1 to 4.2	-	0.35
L01A-3 to L03B-3	0.15	5.2	(+ lead on L01A-3) 25
L01A-6 to L03B-6	0.35	5.3	(+ lead on L01A-6) 27
L01A-7 to L03B-7	-	-	(+ lead on L01A-7) 1.5

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Line input, E04 to E05	93	-	100
Pin 1 to Pin 3	65	-	5.7
Pin 5 to Pin 7	2.5	58	(+ lead on 5) 525

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS3B-1 (-80 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:		RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp.,	CR07-CR12	0.85 to 1.0	0.1 to 0.25	9.5	12.5
Output,	CR01-CR06	23 to 26	-28	7.5	900
Stabilizing,	CR13	-	-	-	-

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	22	(+ lead on R01-1)	310
Bias Setting,	R02	-	0.7	(+ lead on R02-3)	4.0
Cont. Winding,	R03	0.4	39	(+ lead on R03-3)	195
Current Ref. Pri.,	R04	28.0	-		100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds			
Stabilizing,	R07	-	-	(+ lead on R07-3)	

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	93	0.2
Primary 1 to 3	100	0.2
Primary 2 to 3	95	0.2
Secondary A to Neutral	21.6	0.05 Approx.
Secondary B to Neutral	20.3	0.05 Approx.
Secondary C to Neutral	20.0	0.05 Approx.

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	55 to 60	-	1.0	
3 to 4	82 to 90	6.2	30	
5 to 6	82 to 90	5.6	30	
7 to 8	20.5 to 23.8	-	0.7	
L01A-3 to L03B-3	0.4	37	(+ lead on L01A-3)	180
L01A-6 to L03B-6	1.1	34	(+ lead on L01A-6)	180
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	4.5

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	90	-	100	
Pin 1 to Pin 3	62	-	5.4	
Pin 5 to Pin 7	2.1	57.5	(+ lead on 5)	500

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS2A-2 (-100 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:	RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp., CR07-CR12	0 to 1.6	0 to 1.2	3.6	13.2
Output, CR01-CR06	30 to 42	-35	2.6	240
Stabilizing, CR13	-	-	2.9	570

RESISTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Voltage Cont., R01	-	17	(+ lead on R01-1) 350
Bias Setting, R02	-	17	(+ lead on R02-3) 90
Cont. Winding, R03	4.0	72	(+ lead on R03-3) 340
Current Ref. Pri., R04	32	-	100
Capacitor Charging, R05	Shorted out by relay after 20 seconds		
Stabilizing, R07	-	-	(+ lead on R07-3) 190

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	135	1.8
Primary 1 to 3	120	1.8
Primary 2 to 3	125	1.8
Secondary A to Neutral	38.2	0.175
Secondary B to Neutral	35.3	0.175
Secondary C to Neutral	34.2	0.175

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
1 to 2	35 to 70	-	4.2
3 to 4	40 to 80	5.0	24
5 to 6	40 to 80	4.6	24
7 to 8	11 to 20	-	0.65
L01A-3 to L03B-3	4.0	30	(+ lead on L01A-3) 150
L01A-6 to L03B-6	3.9	27	(+ lead on L01A-6) 150
L01A-7 to L03B-7	-	-	(+ lead on L01A-7) 4.2

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Line input, E04 to E05	94	-	105
Pin 1 to Pin 3	64	-	5.7
Pin 5 to Pin 7	3.4	60	(+ lead on 5) 580

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS2A-1 (-150 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:		RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp.,	CR07-CR12	0 to 2	0 to 1	3.3	13
Output,	CR01-CR06	70	-70	2.7	430
Stabilizing,	CR13	-	-	-	-

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Voltage Cont.,	R01	-	11	(+ lead on R01-1) 350
Bias Setting,	R02	-	17	(+ lead on R02-3) 90
Cont. Winding,	R03	0	120	(+ lead on R03-3) 500
Current Ref. Pri.,	R04	32	-	100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds		
Stabilizing,	R07	-	-	(+ lead on R07-3)

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	150	1.8
Primary 1 to 3	146	1.8
Primary 2 to 3	155	1.8
Secondary A to Neutral	61	0.35
Secondary B to Neutral	61	0.35
Secondary C to Neutral	58	0.35

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
1 to 2	40 to 60	-	4
3 to 4	40 to 70	5.0	24
5 to 6	40 to 70	5.0	24
7 to 8	10 to 20	-	0.65
L01A-3 to L03B-3	0	30	(+ lead on L01A-3) 150
L01A-6 to L03B-6	3.6	29	(+ lead on L01A-6) 150
L01A-7 to L03B-7	-	-	(+ lead on L01A-7) 4

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE
Lint input, E04 to E05	95	-	110
Pin 1 to Pin 3	62	-	5.3
Pin 5 to Pin 7	3.0	57	(+ lead on 5) 580

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS2B-1 (-200 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:		RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp.,	CR07-CR12	0.75 to 0.85	0.45 to 0.60	3.1	13.0
Output,	CR01-CR06	98	-96	2.9	520
Stabilizing,	CR13	12.3	- 6.7	2.6	990

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	10.1	(+ lead on R01-1)	320
Bias Setting,	R02	-	20.8	(+ lead on R02-3)	105
Cont. Winding,	R03	0.26	170	(+ lead on R03-3)	770
Current Ref. Pri.,	R04	33	-		100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds			
Stabilizing,	R07	12.2	192	(+ lead on R07-3)	470

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	158	1.5
Primary 1 to 3	158	1.5
Primary 2 to 3	161	1.5
Secondary A to Neutral	88	0.9
Secondary B to Neutral	90	0.9
Secondary C to Neutral	88	0.9

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	40 to 44	-	4.1	
3 to 4	46.2 to 51.2	4.8	24	
5 to 6	46.2 to 51.2	4.7	24	
7 to 8	11.7 to 13.0	-	0.7	
L01A-3 to L03B-3	0.27	28.8	(+ lead on L01A-3)	140
L01A-6 to L03B-6	1.0	28.0	(+ lead on L01A-6)	150
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	3.9

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	96	-	100	
Pin 1 to Pin 3	65	-	5.4	
Pin 5 to Pin 7	1.85	59	(+ lead on 5)	550

TABLE 3. TYPICAL VOLTAGE AND RESISTANCE MEASUREMENTS: POWER SUPPLY PS6A-1 (-300 Volt Unit) (Cont.)

Voltage measurements taken on Triplett Model 630-A meter with B+ set to nominal voltage, no load. Resistance measurements taken on Simpson Model 260 meter with no external connections to the power supply and with the voltage control pot at its maximum counter-clockwise position.

RECTIFIERS:	RMS VOLTAGE	D-C VOLTAGE	FORWARD RESISTANCE	REVERSE RESISTANCE
Mag. Amp., CR07-CR12	0 to 2	0 to 1	1.5	6.0
Output, CR01-CR06	150	-150	1.6	1500
Stabilizing, CR13	-	-	-	-

RESISTORS:		RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Voltage Cont.,	R01	-	17	(+ lead on R01-1)	170
Bias Setting,	R02	-	17	(+ lead on R02-3)	85
Cont. Winding,	R03	0.1	270	(+ lead on R03-3)	1200
Current Ref. Pri.,	R04	47	-		100
Capacitor Charging,	R05	Shorted out by relay after 20 seconds			-
Stabilizing,	R07	-	-	(+ lead on R07-3)	-

POWER TRANSFORMER:	RMS VOLTAGE	RESISTANCE
Primary 1 to 2	170	0.8
Primary 1 to 3	164	0.8
Primary 2 to 3	157	0.8
Secondary A to Neutral	138	1.0
Secondary B to Neutral	141	1.0
Secondary C to Neutral	135	1.0

REACTORS:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
1 to 2	10 to 60	-	2.2	
3 to 4	10 to 75	5.4	26	
5 to 6	10 to 75	5.4	26	
7 to 8	3 to 20	-	0.65	
L01A-3 to L03B-3	0	32	(+ lead on L01A-3)	156
L01A-6 to L03B-6	3.0	32	(+ lead on L01A-6)	156
L01A-7 to L03B-7	-	-	(+ lead on L01A-7)	3.9

CURRENT REF. CIRCUIT:	RMS VOLTAGE	D-C VOLTAGE	RESISTANCE	
Line input, E04 to E05	111	-	100	
Pin 1 to Pin 3	70	-	5	
Pin 5 to Pin 7	3.5	65	(+ lead on 5)	400

BLOWER CABINET MAINTENANCE

1. GENERAL

When mechanical adjustments are being performed in the Blower (90000) Cabinet, the power must be shut off. Access to the fan assemblies is made through doors on the outer sides of the cabinet. Access to the air filters is made by removing the protecting grills from the cabinet. The cooling system controls are shown in Figure 1.

2. FAN ASSEMBLIES

Each of the two fan assemblies consists of a drive motor, a fan, and a V-type belt.

The drive belt between the fan and the drive motor must be under a tension just sufficient to prevent slippage of the belt during normal operation. Belt tension is adjusted by setting the distance between the motor pulley and fan pulley and by using the hinged adjustment bolts provided.

3. BLOWER VANE SWITCHES

Each blower unit has a blower vane switch mounted in the main air duct. If the blower should stop, the switch creates an emergency power shutdown. No maintenance is necessary on these switches.

4. MAINTENANCE OF AIR FILTERS

The cabinet is equipped with eighteen air filters. These filters require periodic cleaning if a full volume of air is to be supplied to the cabinets. The filters should be cleaned whenever a noticeable amount of dirt has accumulated on them.

a. REMOVAL OF FILTERS. - The air filters are arranged in six groups of three each and are located directly behind four protecting grills. These grills may be removed by releasing four machine screws. Each filter is dislodged from its mounting by opening two holding clips on the upper corners of the filter.

b. CLEANING OF FILTERS. - Filters should be cleaned in the following manner.

Step 1. Boil for 30 minutes in a solution of eight ounces of Oakite No. 16 per gallon of water.

Step 2. Rinse in clear, hot water and allow to dry.

Step 3. Spray with light lubricating oil. Take care not to spray so heavily that oil drips from the filter.

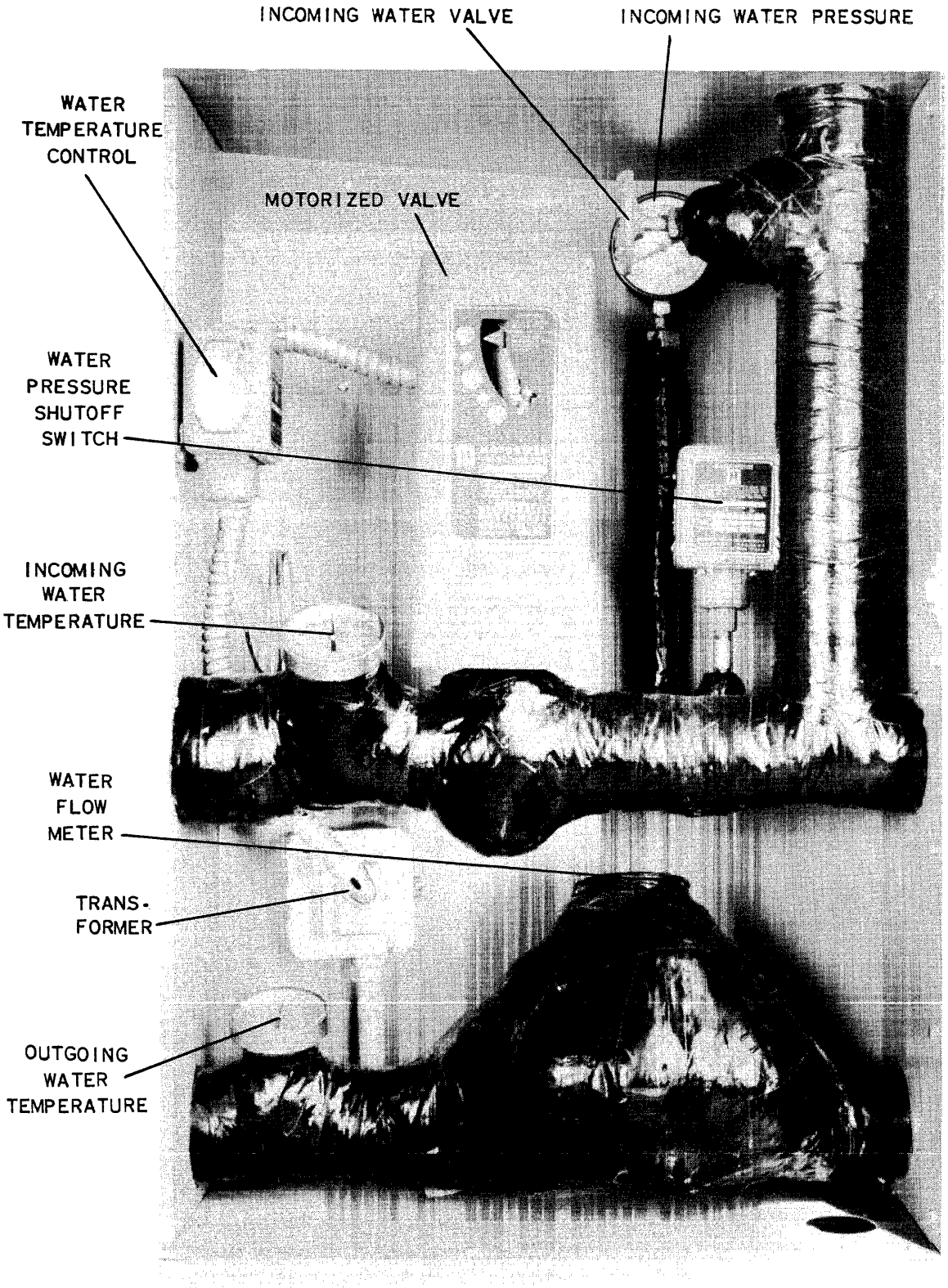

Figure 1. Cooling System Controls

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5. ADJUSTMENT OF TEMPERATURE CONTROLS

The temperature control circuit is a modulating thermostat and motorized valve system (see Figure 1). The modulating thermostat is properly set and tested at the Honeywell factory, and should be returned for readjustment if it does not function properly. The motorized valve requires two adjustments, which can be made as follows.

a. STROKE ADJUSTMENT. - Remove the cover from the motorized valve. With the linkage mounted on the valve, remove the red, white, and blue thermostat wires from the motor. Keep the transformer wired to the motor. Short the red and white terminals on the motor. Loosen the large hex screw on the brass trunnion and set to the desired length of stroke as indicated on the scale above the arm. Then tighten the hex screw.

b. STRAIN RELEASE ADJUSTMENT. - With the red and white terminals still shorted, loosen the hex lock nut below the brass trunnion. Turn the adjustment screw at the top of the spring cage either to right or left until the top of the upper washer is even with the top of the indicator mark on the spring cage. Tighten the lock nut. Remove the red to white short and reconnect the thermostat leads to the motor.

INPUT/OUTPUT EQUIPMENT MAINTENANCE

1. GENERAL

The input/output equipment is a group of self contained units which are compatible with the Central Computer System. These units include standard devices, supplied with the computer, and optional devices, supplied by the customer. Since each unit is self contained, the instruction manual for the device, as prepared by the manufacturer, is supplied with the unit, and the reader is referred to the maintenance section of that manual for the necessary procedure.

The standard input/output devices are mounted on the Operator's Desk and include the Photoelectric Tape Reader, the High-Speed Punch, and the Output Typewriter.

The optional input/output devices include such items as the Magnetic Tape Storage System, the Univac High-Speed Printer, and the Controlled Reproducer.

Interconnections between the input/output equipment and the Central Computer System are made through a Diode Board and/or Junction Board.

2. FERRANTI PHOTOELECTRIC TAPE READER MAINTENANCE

The adjustments for the tape reader are shown in Figure 1. Maintenance of this device is described in detail in the Ferranti Reader Service Manual supplied with the equipment.

3. HIGH-SPEED PUNCH MAINTENANCE

Figures 2, 3, and 4 show views of the High-Speed Punch with the cover removed. Maintenance of this device consists primarily in the periodic emptying of punchings from the drawer in the bottom of the punch, the lubricating of moving parts, and the replacing of blank paper tape.

The replacement of parts and adjustment procedures are described in detail in Teletype* Bulletin 215B, supplied with the equipment.

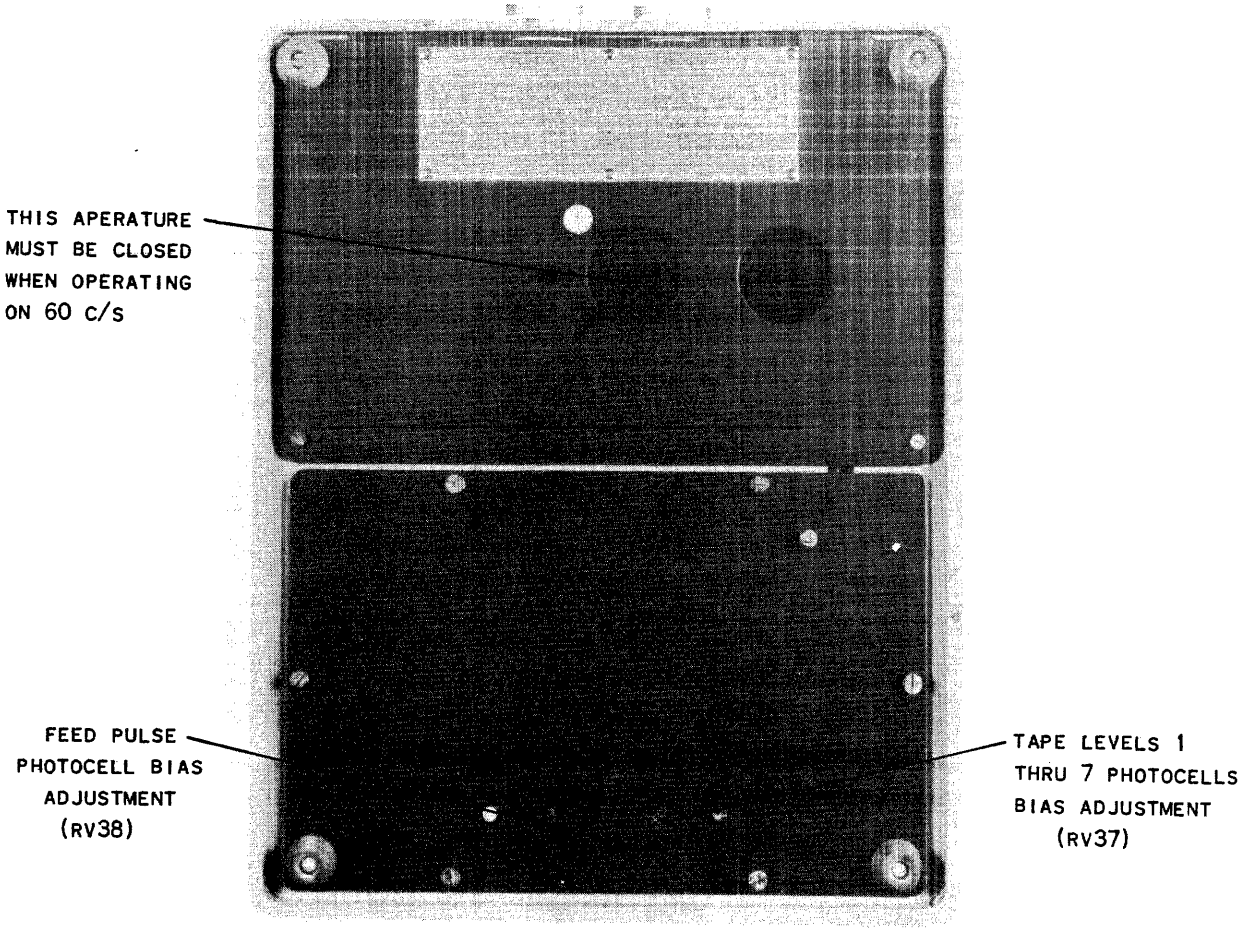
4. TYPEWRITER MAINTENANCE

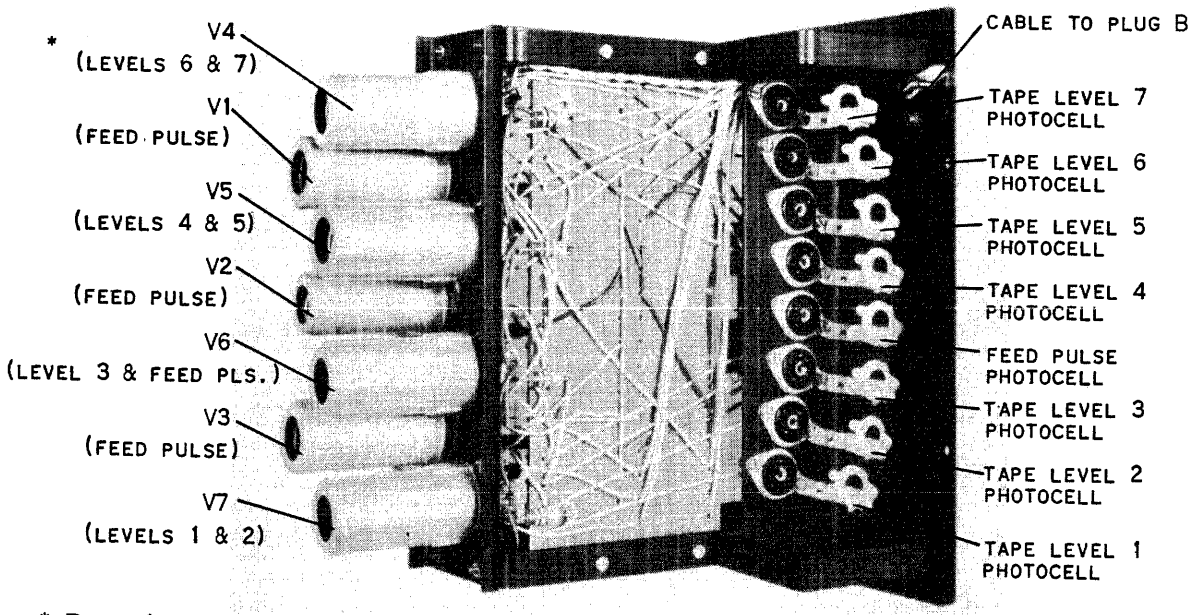
The Output Typewriter is shown in Figure 5. The maintenance of this device is described in detail in the Flexowriter Service Manual, supplied with the equipment.

5. OPTIONAL EQUIPMENT MAINTENANCE

The maintenance procedures for an optional input/output device are contained in the volumes prepared for that equipment. The reader must reference the maintenance section of these volumes for the necessary information.

*Registered Trade Mark, Teletype Corp.





*** Parenthetical notes indicate only the circuit associated with each tube**

Figure 1. Ferranti High-Speed Tape Reader Adjustments
PX 136

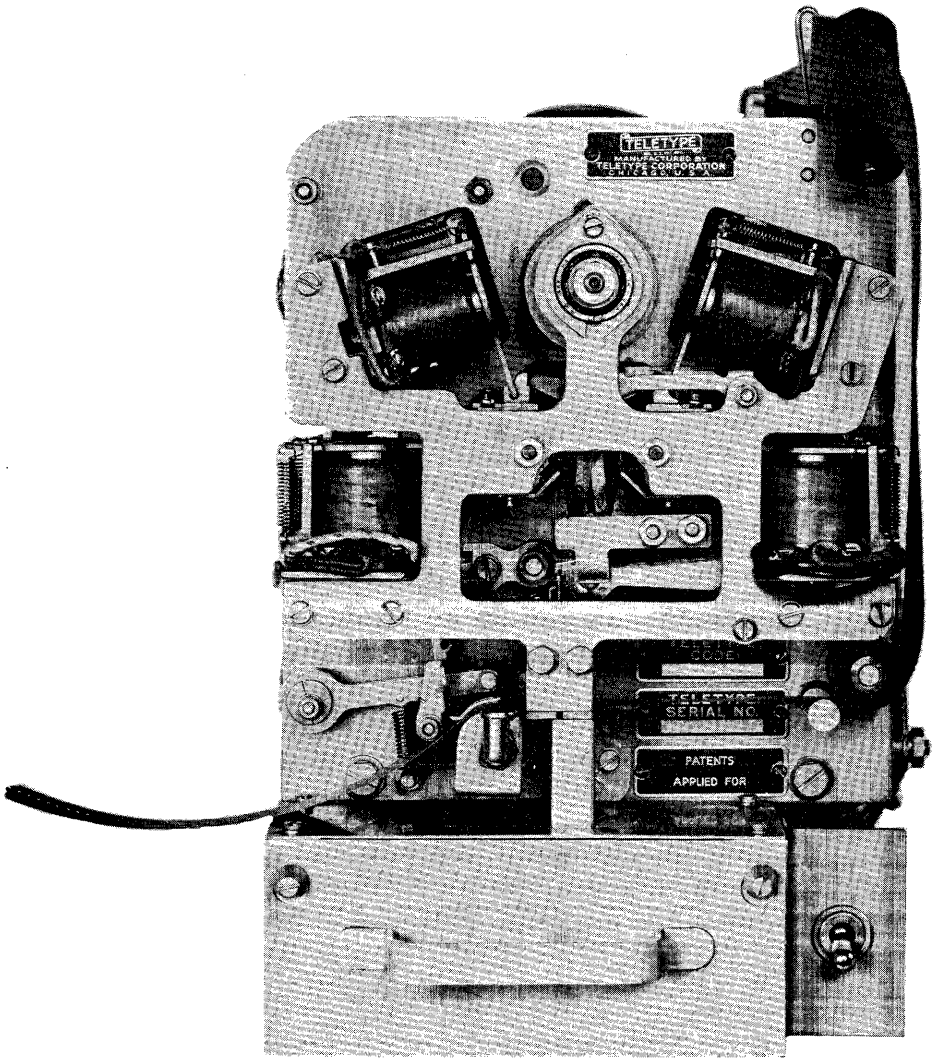


Figure 2. High-Speed Punch With Cover Removed, Front View
PX 136

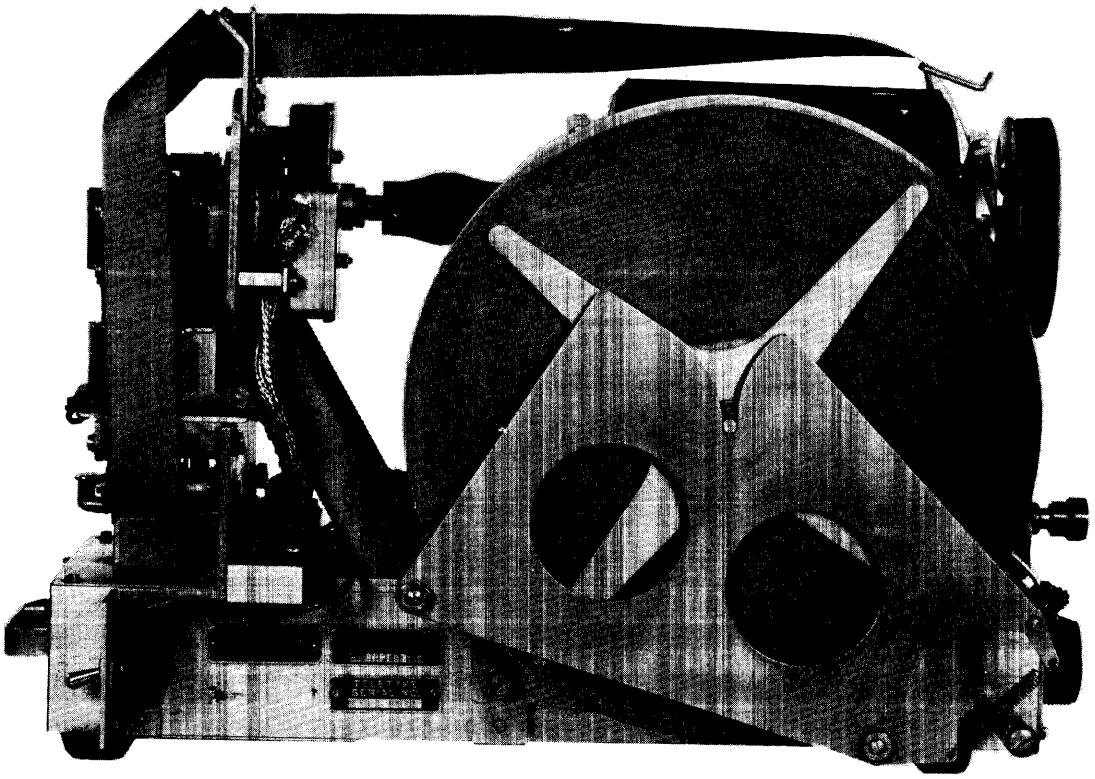


Figure 3. High-Speed Punch With Cover Removed, Side View
PX 136

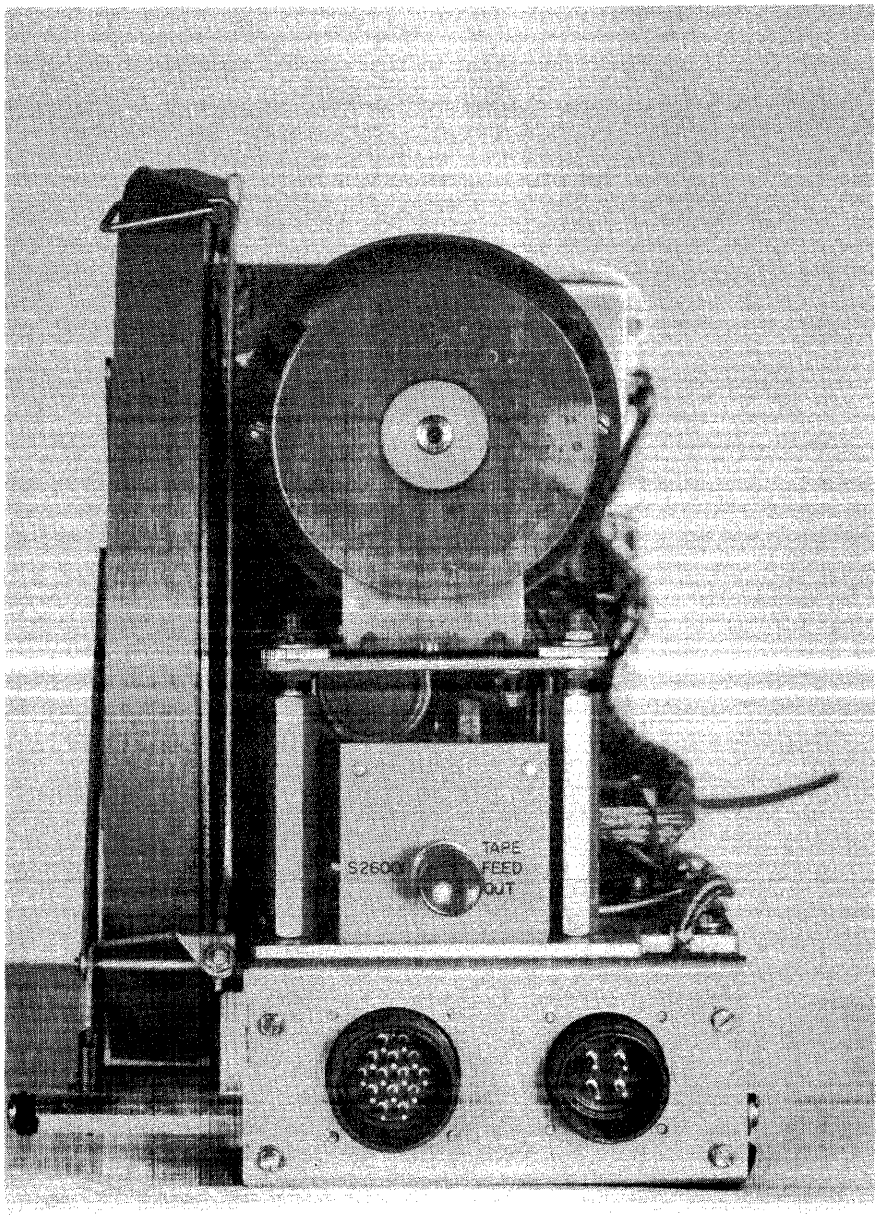


Figure 4. High-Speed Punch With Cover Removed, Rear View
PX 136

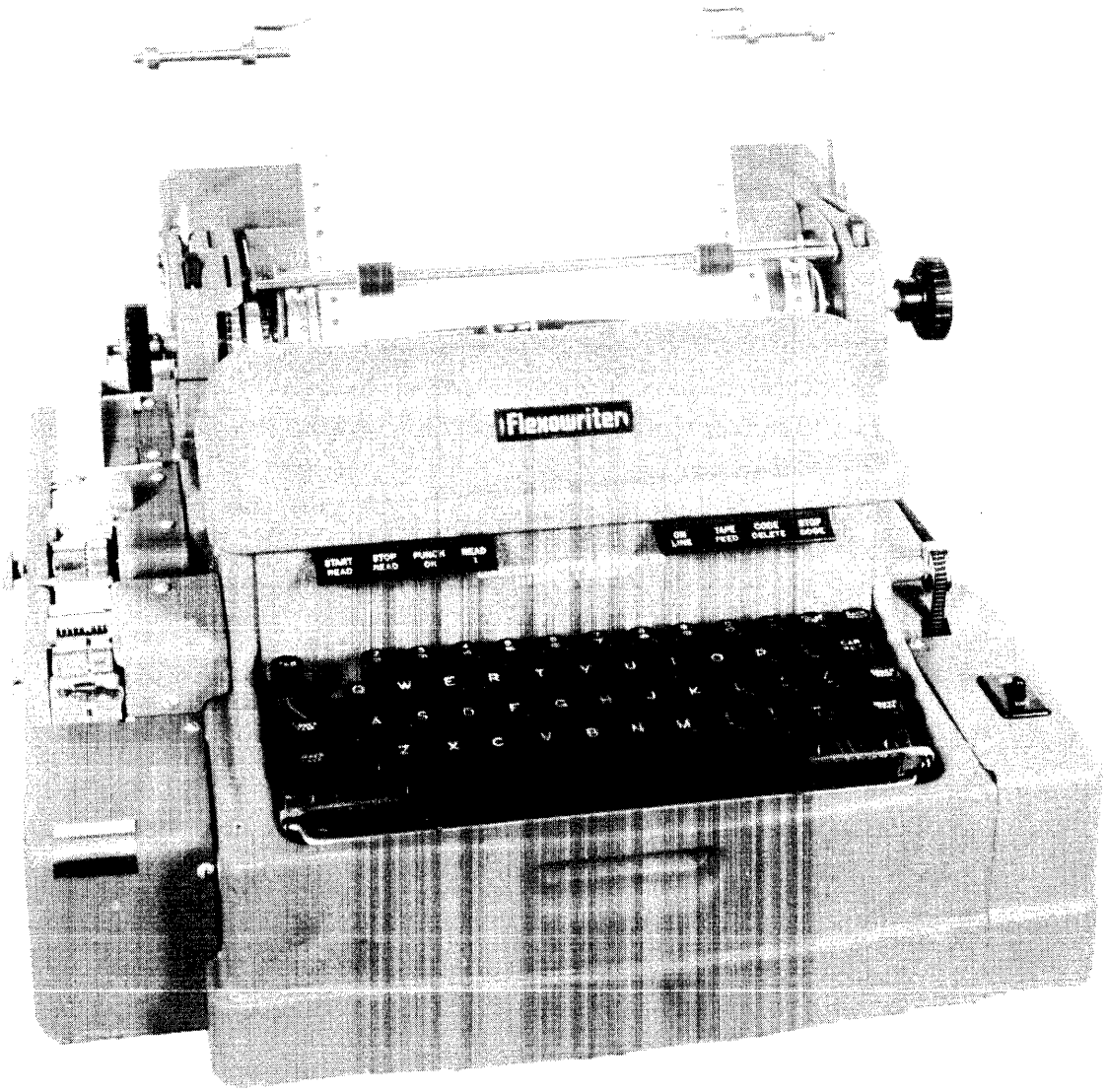


Figure 5. Electric Typewriter
PX 136

6. DIODE BOARD MAINTENANCE

The diode board (E40501 through E40505), located in the rear of the Supervisory Control Cabinet, houses the diodes used for isolating external equipments. Maintenance on this board will consist of the replacement of malfunctioning diodes.

7. JUNCTION BOARD MAINTENANCE

The junction board, shown in Figure 6, is located beneath the porch adjacent to the Operator's Desk. External equipment is connected to the central computer by inserting the plug associated with the external equipment into the appropriately labelled jack on the junction board. Maintenance is required only on wiring connections.

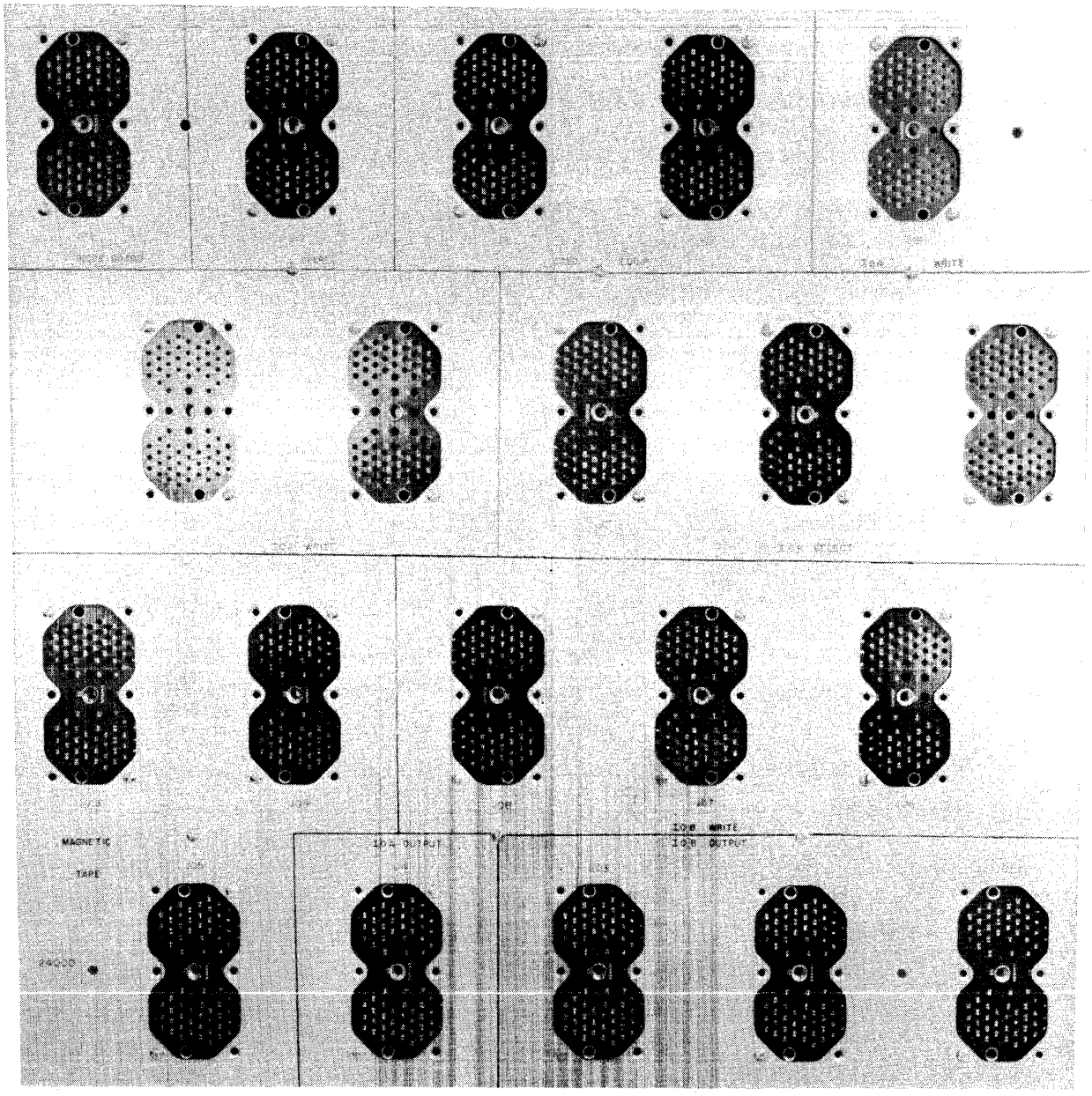


Figure 6. Junction Board
PX 136

LUBRICATION

1. BLOWER SHAFT BEARING

The grease cups provided for the right and left bearings should be removed every three months and refilled with Navy Type 14G1 Grade II grease or its equivalent. To insure continuous lubrication, the grease cups should be given one complete turn downward after each 40 hours of operation. Every 15,000 to 20,000 hours, caked grease should be removed from the bearings. To clean the bearings, remove the grease fittings, fill the bearings with flushing oil (or kerosene), and run the blower for fifteen minutes. Shut off the blower and remove the drain plugs and grease fittings. Add grease to the fittings until the bearings are approximately half full.

2. BLOWER DRIVE MOTOR

The blower drive motor is sealed and requires no lubrication.

3. DRUM ASSEMBLY

The drum bearings are packed with grease at the time of assembly and require no lubrication. After five years of operation or 25,000 hours, whichever occurs first, the drum should be returned to the manufacturer for relubrication.

4. DRUM DRIVE MOTOR

The drive motor is a 3/4 hp, 220vac motor equipped with single-seal ball bearings, and, before leaving the factory, it is properly lubricated for two years of normal service. After two years the motor should be relubricated at approximately one-year intervals, using one or two cc of high-grade, neutral, medium-consistency ball-bearing grease.

5. TAPE READER

Complete lubrication instructions for the Ferranti Tape Reader are given in detail in the Ferranti Instruction Manual supplied with the equipment.

6. MOTORIZED VALVE

To lubricate the motorized valve, apply Lubriplate to all moving parts. This should be done twice a year for normal applications, but should be done more frequently if the location is very warm or if the valve operates very frequently.

7. HIGH-SPEED PUNCH

Because the High-Speed Punch is a precision device with many rapidly moving parts, it should be kept well lubricated. A very detailed lubrication procedure is described in Teletype Bulletin 215B, supplied with the equipment.

8. EXTERNAL EQUIPMENT

The lubrication procedures for optional input/output equipment, such as the Magnetic Tape Storage System and the Univac High-Speed Printer, is included in the volumes prepared for this equipment. It is important that these volumes be referenced to get the proper lubrication procedures.

MAGNETIC HEAD SETTING

No adjustment of the magnetic heads should be attempted. At the time the equipment is installed, the magnetic heads are properly positioned, and, if further adjustments are necessary, qualified manufacturer's personnel will visit the installation to make the necessary adjustments.

MAGNETIC DRUM ERASE PROCEDURE

1. GENERAL

Erasure of data may become necessary in the event of an equipment power failure, causing information to be recorded between the regular circumferential storage positions on the drum tracks. This condition results in a timing derangement that must be corrected before storage positions can be properly addressed.

To place tracks of the magnetic drum in a neutral state, an alternating current is applied to the head tracks with the use of the Drum Erase equipment (28500 unit) supplied with the computer. The erasing operation must be performed with all of the equipment power on and the drum rotating.

Two procedures are described below. The first procedure describes the method of erasing only one drum track, and the second describes the method of erasing the entire drum. Special precautions must be taken to prevent the erasure of the Timing Track or the Mark Track. The cable from the Drum Erase equipment must never be connected to the Timing Track head, the Mark Track head, or any of the spare heads storing spare timing tracks or mark tracks.

2. PROCEDURE FOR ERASING ONE TRACK

Step 1. Connect cable W28501 (which has a five-contact connector on each end) to the jack on the Drum Erase equipment.

Step 2. Connect the power cord to 110vac.

Step 3. Set the toggle switch to the ON position. The neon indicator should glow.

Step 4. Connect cable plug P04 to the magnetic head positioned over the track to be erased.

WARNING

NEVER CONNECT PLUG P04 TO THE TIMING TRACK HEAD, THE MARK TRACK HEAD, OR ANY OF THE SPARE HEADS STORING SPARE TIMING TRACKS OR MARK TRACKS.

Step 5. Press the black START button. Immediately the meter should register one ampere. The meter reading slowly reduces to 0 ampere in about 15 seconds.

Step 6. Reconnect the drum head cable to the head, and check the output of the read circuit with an oscilloscope. If the track is not completely erased, repeat steps 4 through 6.

3. PROCEDURE FOR ERASING ALL TRACKS

Step 1. Connect cable W28502 (which has a 74-pin connector on one end) to the Drum Erase equipment.

Step 2. Connect the power cord to 110vac.

Step 3. Set the toggle switch to the ON position. The neon indicator should glow.

Step 4. Remove Read-Write Amplifier Chassis number 0 from J60174 (located in the 60000 Cabinet).

Step 5. Insert the 74-pin plug of cable W28502 into J60174.

Step 6. Press the black START button. Immediately the meter should register one ampere. The meter reading is slowly reduced to 0 ampere in about 15 seconds.

Step 7. Disconnect the 74-pin plug and replace the Read-Write Amplifier chassis in J60174.

Step 8. Repeat steps 4 through 7 for the remaining 35 Read-Write Amplifier chassis in the 60000 Cabinet.

4. PROCEDURE FOR ADJUSTING THE DRUM ERASE EQUIPMENT

If the neon indicator does not glow, check the fuses in the twist-lock fuse holders.

If the maximum current reading is not one ampere when one head is being set, connect a spare head to the equipment, lay the equipment on its side, and perform the single-track erase procedure while adjusting potentiometer R02, located inside the chassis. Adjust this potentiometer until a maximum meter reading of one ampere is obtained.

If the maximum meter reading is not one ampere while the 74-pin plug cable is being used, lay the equipment on its side, and adjust potentiometer R01 while repeating the drum erase procedure. Adjust for a maximum meter reading of one ampere.

DATA HANDLING ROUTINES

1. GENERAL

The data handling routines are independent routines utilized in the manipulation of information. Through these routines an operator may load information into the computer, print the contents of a selected set of storage addresses, reproduce on paper tape a particular stored program, or transfer a stored program to a new storage location.

Many data handling routines may also be used as subroutines of another program. For example, the type text routine may be used as a subroutine of a test program to type out information concerning the progress of the test.

The routines discussed here include only the loading routines. The other data handling routines are described in the volume on supplementary maintenance routines.

2. THE FERRANTI READER LOADING ROUTINE

The Ferranti Reader Loading Routine is used to load information into the computer from a tape employing standard seventh level coding. The routine, stored in the drum reserve space, is transferred to MC addresses 00000 through 00041 by MASTER CLEARING, setting the MD switch to ABNORMAL, and pressing the START button. To initiate the loading sequence, set the Reader to ON, set the MD switch to NORMAL, and press the START button. (See Figure 1.)

Instruction 00000 (F_1) is a jump instruction. The first execution of this instruction merely produces a jump to 00006, the first step of the Ferranti loading cycle.

Each performance of the loading cycle processes one tape frame. If MJ3 is selected, the repeated execution of this cycle causes the tape reader to run continuously; if MJ3 is not selected, the tape "steps", i.e., the reader momentarily stops after each 36-bit tape word. Each performance of this cycle inserts the six data bits from the tape frame into a 36-bit "word assembly", inserts the seventh-level tape bit into a seven-bit "instruction code assembly", then performs an Insert Address, Enter Data, or Check Address operation, depending upon the seventh-level tape coding.

In the cycle, External Function instruction 00006 starts the tape reader. Next, External Read instructions 00007 reads one tape frame, consisting of seven bits, into Q. Instructions 00010 and 00011 perform masking operations which isolate the six data bits and shift them into the lower-order six stages of the "word assembly" in address 00035. The operation is performed in a manner such that the "word assembly" contains the currently-read six bits in stages 0 through 5, the previously-read six bits in stages 6 through 11, etc., so that at the end of every six cycles, a completely assembled 36-bit tape data word is present in 00035. Instructions 00012 through 00014 perform similar masking and assembly operations on the seventh-level bits, so that the "instruction code assembly", in the lower-order seven stages of 00036, always contains an image of seven adjacent seventh-level holes on the tape.

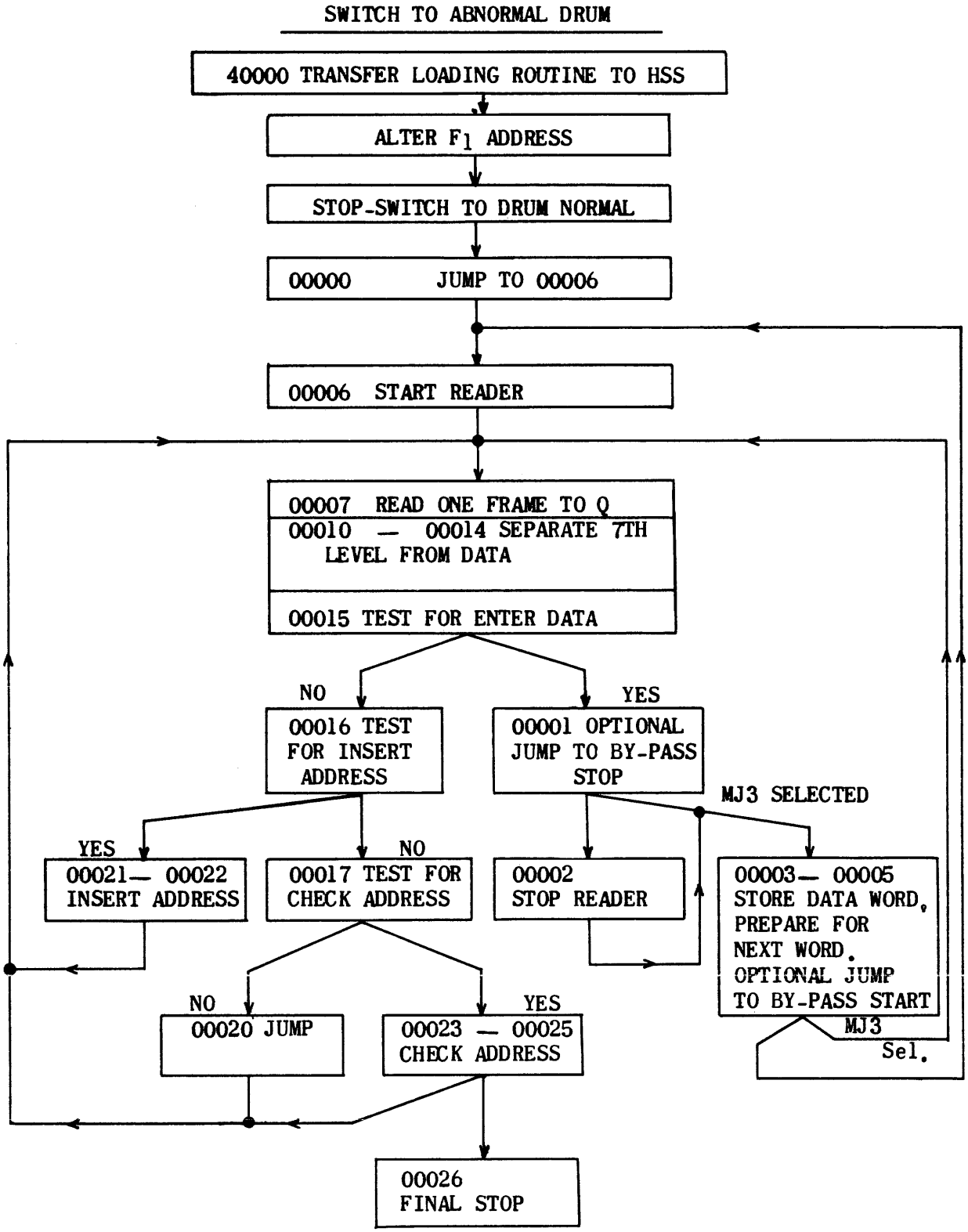


Figure 1. Ferranti Reader Loading Routine
PX 140

During each cycle, a branched series of instructions perform checks on the current "instruction code assembly" word. The sequence of operations occurring during the loading of the tape is as follows.

a. INSERT ADDRESS. - Because the first entry on the tape is an Insert Address word, instructions 00015, 00016, 00017, and 00020 are executed during the first five cycles; then during the sixth cycle, after the sixth frame is read, instructions 00015, 00016, 00021, and 00022 are executed. Instruction 00021 inserts the proper 15-bit loading address (obtained from the tape and assembled in 00035) into Transmit Positive instruction 00003, which performs data word loading.

b. ENTER DATA. - After the Insert Address operation, instructions 00015, 00016, 00017, and 00020 are executed for five more cycles; then, in the sixth cycle, instructions 00015, 00001, 00002 (optional), 00003, 00004, 00005, and 00006 (optional) are executed, due to the Enter Data code present after each 36-bit data word on the tape. Instruction 00003 causes the 36-bit word in the "word assembly" to be transferred to a particular storage address, then instruction 00004 advances the v-portion of instruction 00003 so that the next word will be inserted into the next storage address. Thus, the 36-bit data words are loaded into consecutive addresses, starting with the address specified by the Insert Address Operation. Instructions 00002 (stop reader) and 00006 (start reader) are optional, and are not executed if MJ3 is selected.

c. CHECK ADDRESS. - After all data words have been loaded, the final entry on the tape is a Check Address code and address. Thus five cycles are performed which execute instructions 00015, 00016, 00017, and 00020; then a final sixth cycle is performed which executes 00015, 00016, 00017, 00023, 00024, and 00025. The latter three instructions check the v-address portion of instruction 00003 with the check address in 00035 to see if the last data word was stored in the proper address. If the word is stored properly, 00025 executes a jump to 00007, so that the tape continues to run through the reader. If the check fails, Final Stop instruction 00026 is executed, and the Supervisory Control Panel selections drop.

It should be noted that this routine can also be used for tapes which contain no Insert and Check Address coding. If the routine is used in this manner, the first data word is loaded into address 40000.

3. THE FRI-2 LOADING ROUTINE

The FRI-2 Loading Routine is used to load information into the computer from a tape employing standard seventh level coding. Basically FRI-2 is a Ferranti loading routine which has been modified to (1) Increase loading efficiency by first loading to high speed storage, then block transferring to final storage, (2) Reproduce paper tape which is being loaded, and (3) Reproduce paper tape and punch computed check-sums after each check address. The reproduce feature has been added to facilitate the reproduction of very long maintenance tapes, and is especially useful when it is desired to take advantage of the check-sum feature of FRI-2. By selecting appropriate stops and jumps, information may be added to, or deleted from, an existing tape. The check-sum and check address tests stop the loading operation in the event of a feed pulse failure or if the reader fails to read, or adds, one or more bits. (See Figure 2.)

TABLE 1. FERRANTI READER LOADING ROUTINE

PROGRAM: Ferranti Reader Loading Routine

DESCRIPTION: For use with tape employing standard seventh level coding. The routine is stored in the drum reserve space and is transferred to MC addresses 00000 thru 00041 by MASTER CLEARING, setting the MD switch to ABNORMAL (up), and pressing the START button. The loading may then be initiated by setting the Reader to ON, setting the MD switch to NORMAL (down), and pressing the START button.

Select MJ3 to bypass "stop reader" instructions during the enter data operation.

ADDRESS	OP-CODE	U	V	FUNCTION
40000	75	30010	40002	Transfer test to MC
40001	11	40400	00000	
40002	75	30010	40004	
40003	11	41000	00010	
40004	75	30010	40006	
40005	11	41400	00020	
40006	75	30012	40010	
40007	11	42000	00030	
40010	11	40410	00000	Transmit jump to F_1 address
40011	56	00000	00006	STOP, shift to drum NORMAL-jump to load
40410	45	00000	00006	Jump for F_1 address
40400 thru 40407				See 00000 thru 00007
41000 thru 41007				See 00010 thru 00017
41400 thru 41407				See 00020 thru 00027
42000 thru 42011				See 00030 thru 00041
00000	45	00000	40002	Jump for F_1 address
00001	45	30000	00003	Optional jump to bypass start
00002	17	00000	00040	Stop reader
00003	11	00035	40000	Enter data
00004	21	00003	00037	Advance address
00005	45	30000	00007	Optional jump to bypass start
00006	17	00000	00041	Start reader
00007	76	00000	31000	Read to Q
00010	31	00035	00006	Isolate data levels
00011	52	00027	00035	
00012	31	00036	00001	
00013	52	00030	31000	Isolate seventh level
00014	51	00030	00036	
00015	43	00032	00001	Test for enter data
00016	43	00031	00021	Test for insert address

TABLE 1. FERRANTI READER LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00017	43	00033	00023	Test for check address
00020	45	00000	00007	Jump to continue word assembly
00021	16	00035	00003	Insert address
00022	45	00000	00007	Jump to begin word assembly
00023	11	00003	32000	}
00024	36	00034	32000	
00025	43	00035	00007	} Check address
00026	57	77777	77777	Final stop on failing check address
00027	00	00000	00077	Data levels mask
00030	00	00000	17700	Seventh level mask
00031	00	00000	11100	Insert address code
00032	00	00000	10100	Enter data code
00033	00	00000	10500	Check address code
00034	11	00035	00000	Constant for check address
00035	--	-----	-----	Word assembly
00036	--	-----	-----	Instruction code assembly
00037	00	00000	00001	Constant for advance address
00040	10	00001	00000	Stop reader code
00041	10	00002	00000	Start reader code

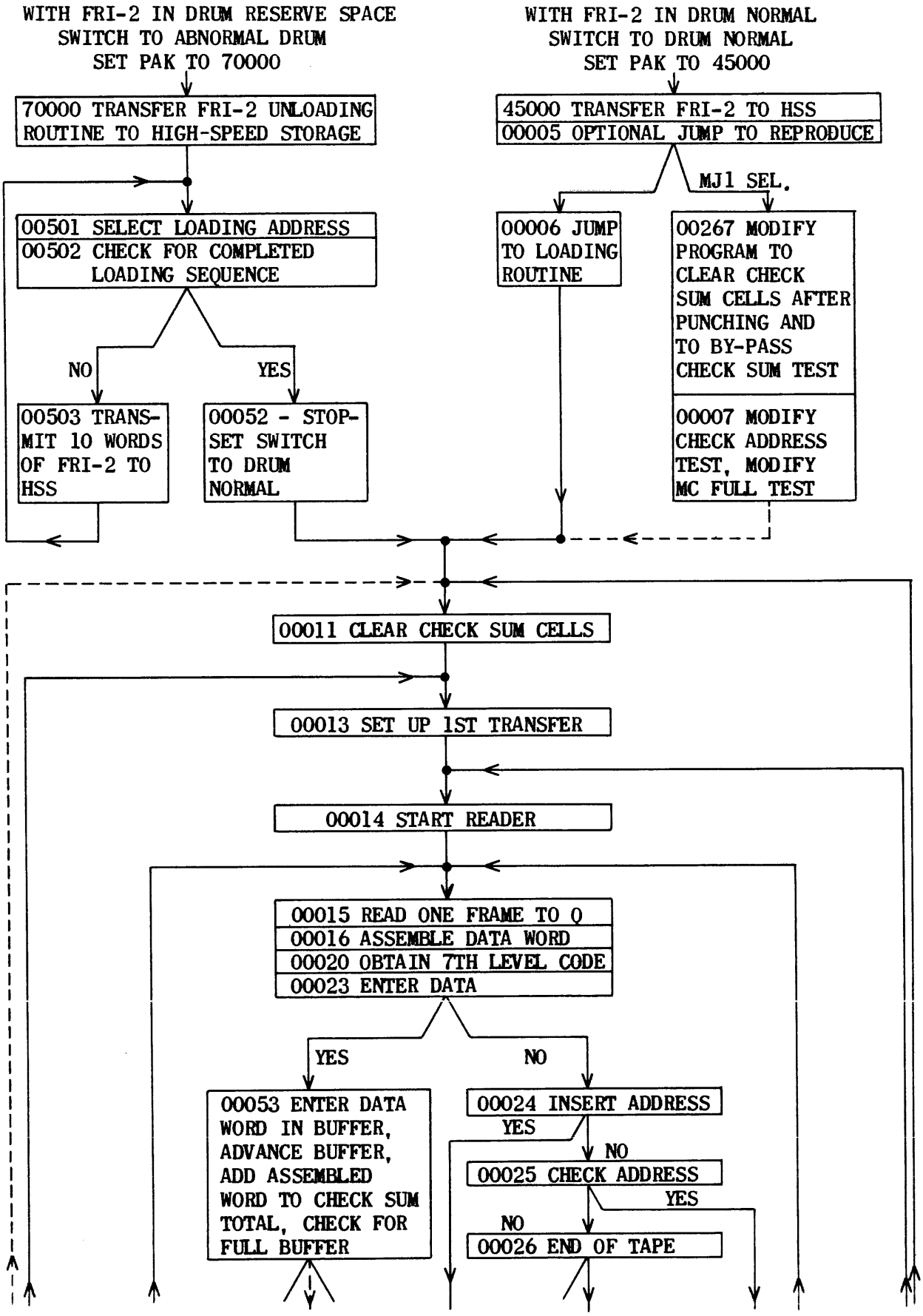


Figure 2. FRI-2 Loading Routine
PX 140

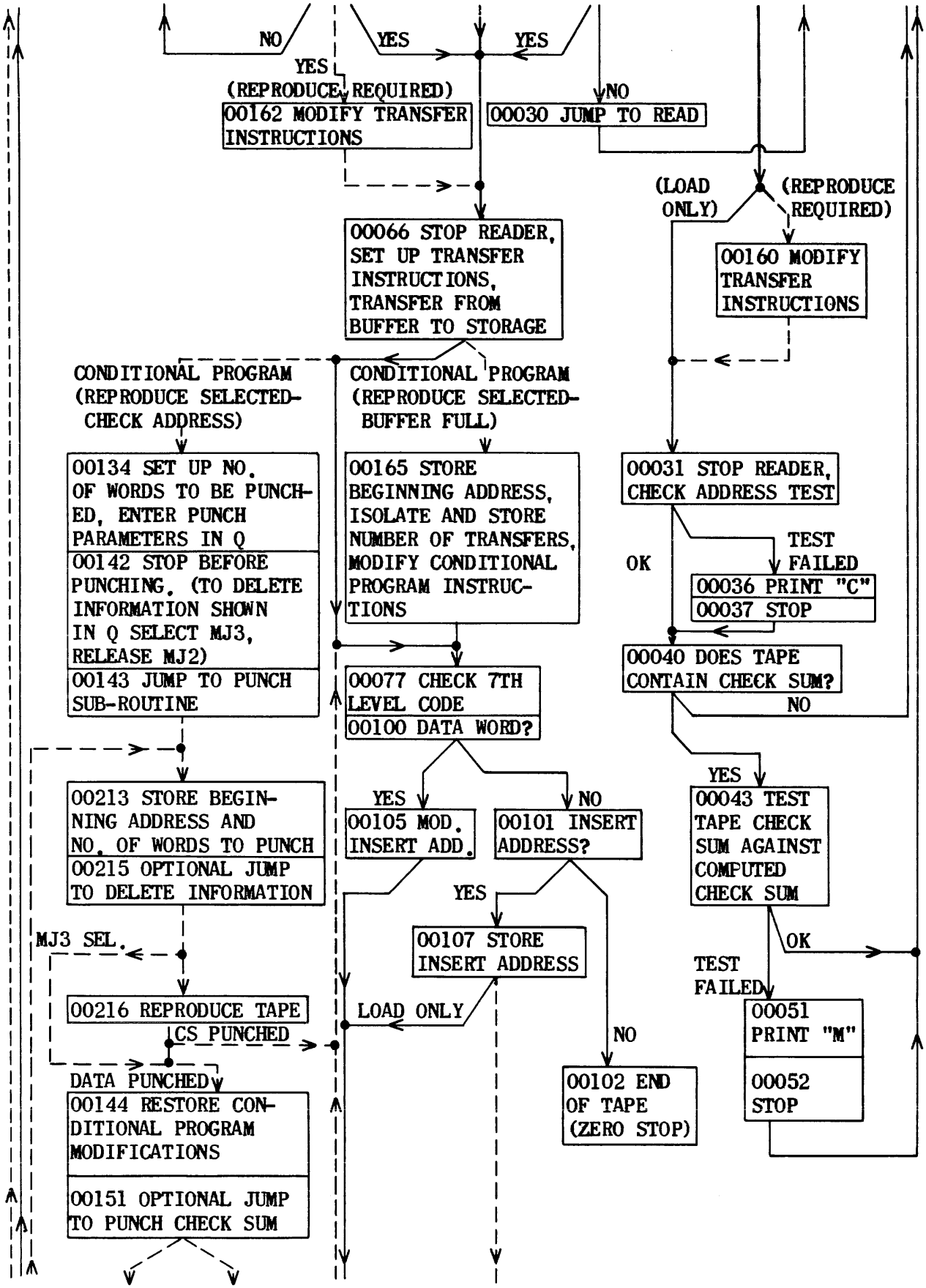


Figure 2. FRI-2 Loading Routine (Cont.)
PX 140

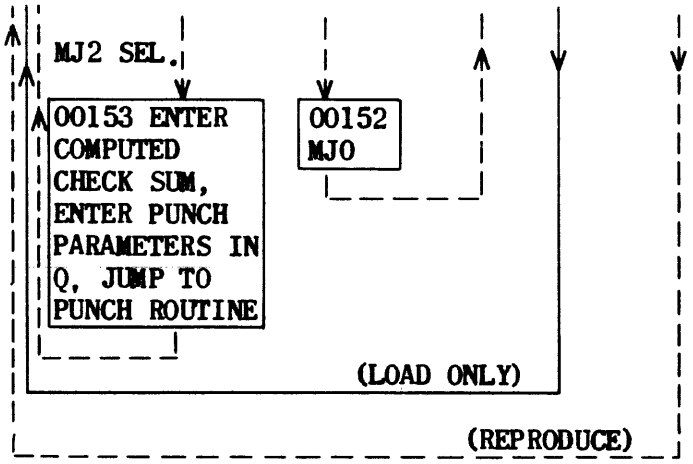


Figure 2. FRI-2 Loading Routine (Cont.)
PX 140

A FRI-2 load only routine is stored permanently in the drum reserve space. The entire routine, including the reproduce feature and check-sum feature, is contained on tape and is temporarily stored on the drum (45000 to 45276) during maintenance test runs.

a. PROCEDURE. - To load only, using the FRI-2 routine stored in the drum reserve space, make the following settings and selections.

Step 1. Set the toggle switch labelled DRUM to the ABNORMAL (up) position.

Step 2. Set PAK to 70000.

Step 3. Press the START button.

The procedure initiates the transfer of the FRI-2 load only routine from the drum reserve space to high speed storage. A zero stop is produced after completion of the transfer, and the loading of tape is initiated thereafter by proceeding as follows:

Step 4. Thread tape in the Reader.

Step 5. Set the Reader to ON.

Step 6. Set the toggle switch labelled DRUM to the NORMAL (down) position.

Step 7. Press the START button.

To load tape, using the FRI-2 routine with the reproduce, and add check sum feature, proceed as follows:

Step 1. Load the FRI-2 routine contained on a tape into the computer using the loading procedure designated in steps 1 through 7 above.

Step 2. Set PAK to 45000 (after the FRI-2 routine has been loaded).

Step 3. Select desired jumps and stops as follows:

1. NONE - to load only,
2. MJ1 - to load and reproduce tape,
3. MJ2 (and MJ1) - to load, reproduce and add check sum,
4. MS1 (and MJ1) or MS1 (and MJ1 and MJ2) - to stop before punching and for punch parameters to appear in Q,
5. MJ3 (and MJ1 and MS1) not MJ2 - to delete information shown in Q (select MJ3 after MS1 then release MJ2),

6. Thread tape in Reader and set Ferranti Reader to ON,

7. Press START button.

Since MJ1 controls all stops and jumps, it must be selected to initiate the optional programs which other stops or jumps are to control.

8. On a check address or check sum failure, press the START to resume the program.

9. To add blocks of data, reset PAK to 45000 after MS1, enter tape in reader and press START.

10. If the tape being loaded is not concluded by a double seventh level code, the computer will hang up on a "76", and a restart at PAK=00066 must be initiated to successfully conclude the routine.

b. THEORY OF THE LOADING ROUTINE. - The initial instructions transfer the program from drum to high-speed storage, then produce a jump to the program in high-speed storage. If MJ1 has been selected, a jump is produced to a modifying sub-routine that alters the jump outs from the full buffer and check address tests, then produces a jump to the loading routine.

The loading routine assembles the information read from tape, inserts the words in buffer storage, then block transfers the buffer contents to final storage.

In the assembly of information, a single tape frame is read to Q, the data bits are separated from the seventh level by a masking operation and shifted into the lower order six stages of the "word assembly" address. Similar masking operations are performed on the seventh level bit and assembled in the "instruction code" address. The seventh level code is then checked for an insert address, enter data, check address, or end of tape.

Since six frames of tape are required to assemble a complete word, the above operation will be repeated five times. On the sixth cycle, an operation dictated by the seventh level "instruction assembly code" produces an insert address, enter data, check address, or end of tape transfer.

On an insert address, a jump is produced to the transfer routine, the reader is stopped, transfer instructions are set up, and the buffer contents transferred to storage. If MJ1 has been selected and a check address has occurred, a jump is produced to the punch routine. If MJ1 has not been selected or a check address has not occurred, the punch routine is by-passed and the seventh level code is rechecked. The insert address is then stored for future reference, and a jump is produced to continue the loading routine.

On an enter data code, the assembled word is transferred to buffer storage, the buffer storage address advanced so that the next word will be loaded in the next address, the word is added to the check sum total and the buffer checked for a full buffer. If the buffer is not full, a jump is executed to continue reading tape. If the buffer is full, a jump is produced to the transfer routine,

the buffer to storage transfer completed, and the seventh level code checked as before. The insert address is modified to establish a new beginning address for the next buffer to storage transfer, and a jump is then produced to continue the loading sequence.

If MJ1 has been selected and a full buffer occurs, the jump out from the buffer to storage transfer is altered to produce a jump from the transfer routine to a subroutine in which the beginning address and number of words transferred are computed and stored for future reference in reproducing the tape. The seventh level is then checked as before, the insert address modified, and a return jump executed to continue reading tape.

On a check address, a jump is produced to the check address test, where the reader is stopped and the check address test executed. If a failure occurs, a "c" is printed and a stop produced. If no failure occurs, the tape is checked for a check sum total and the tape check sum compared with the computed check sum. If a failure occurs, an "m" is printed and a stop produced. If no failures occur, a return jump to continue reading is executed. If the tape does not contain a check sum, a jump is produced directly to the reading cycle.

On a check address with MJ1 selected, a jump is executed to a modifying routine, and the transfer instruction is altered, thus enabling the punch routine to be initiated following the buffer to storage transfer initiated by an insert address or end of tape code.

An end of tape code initiates a final buffer to storage transfer, then produces an end of tape (zero) stop.

The punch routine first sets up the number of words to be punched, enters the punch parameters in Q, then produces a zero stop if MS1 is selected. (The operator may now delete information contained in Q by selecting MJ3 and releasing MJ2.) If MJ3 is not selected, a jump is then produced to the punch routine, and the contents of address in which the tape information was stored are punched on tape.

The conditional program instructions are then restored, and, if MJ2 has been selected, the computed check sum is entered and the check sum punched. Whether or not the check sum is punched, the seventh level is then checked for an insert address or end of tape code. If the punch routine was initiated by an insert address, a jump to continue reading tape is executed. If an end of tape code initiated the punch routine, a final stop is produced.

TABLE 2. FRI-2 LOADING ROUTINE

PROGRAM: FRI - 2. LOADING ROUTINE

DESCRIPTION: Loads information contained on tape employing standard seventh level coding, and, with selection of appropriate stops and jumps, reproduces the tape being loaded, and punches a computed check sum total.

ADDRESS	OP-CODE	u	v	FUNCTION
45000	11	45003	00000	Block Transfer to MC
45001	75	30274	00005	
45002	11	45004	00001	
45003 thru 45276				See 00000 thru 00273
00000	45	00000	00000	
00001	00	00000	00000	Beginning address (V)
00002	00	00000	00000	Number of addresses (Mk)
00003	10	00002	00000	Start Reader Code
00004	10	00001	00000	Stop Reader Code
00005	45	10000	00267	MJ1 to reproduce tape
00006	45	00000	00011	MJØ to load tape
00007	16	00174	00025	Modify check address test
00010	16	00175	00064	Modify "MC full" test
00011	23	00131	00131	Clear check-sum cells
00012	23	00132	00132	
00013	11	00112	00053	Set-up first transfer
00014	17	00000	00003	Read PT to Q
00015	76	00000	31001	

TABLE 2. FRI-2 LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00016	31	00133	00006	Assemble data
00017	52	00113	00133	
00020	31	00114	00001	Obtain seventh level code
00021	52	00116	31016	
00022	51	00116	00114	
00023	43	00117	00053	Test for ED, IA, or CA
00024	43	00120	00066	
00025	43	00121	00031	
00026	51	00122	32007	Test for end-of-tape
00027	43	00122	00066	
00030	45	00000	00015	Return to read
00031	17	00000	00004	Stop reader
00032	11	00053	32000	Check address test
00033	36	00112	32000	
00034	21	32000	00115	
00035	43	00133	00040	
00036	61	00000	00021	
00037	56	00000	00040	
00040	11	00133	32000	Does tape contain CS
00041	43	00123	00043	
00042	45	00000	00014	
00043	31	00131	00044	Tape CS tested against computed CS
00044	32	00132	00000	
00045	34	00300	00000	

TABLE 2. FRI-2 LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00046	34	00301	00000	Tape CS tested against computed CS
00047	34	00301	00044	
00050	43	00300	00011	
00051	61	00000	00026	
00052	56	00000	00011	
00053	11	00133	00300	Enter data word into Buffer
00054	21	00053	00124	Advance buffer address
00055	31	00131	00044	Add assembled word to CS total
00056	32	00132	00000	
00057	32	00133	00000	
00060	11	32000	00132	
00061	54	32000	00044	
00062	11	32000	00131	
00063	11	00053	32000	Is buffer filled with data?
00064	43	00125	00066	
00065	45	00000	00015	Return to read
00066	17	00000	00004	Stop reader
00067	31	00053	00000	Set up number of words to transfer from buffer
00070	34	00112	00017	
00071	35	00126	00075	
00072	11	00115	32000	Is data destined for MC?
00073	42	00127	00103	
00074	16	32000	00076	Enter first transfer address
00075	75	30000	00077	Transfer from buffer to storage
00076	11	00300	00000	

TABLE 2. FRI-2 LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00077	11	00114	32000	Enter seventh level code
00100	43	00117	00105	Test for data word
00101	43	00120	00107	Test for IA
00102	56	00000	45000	End of tape
00103	21	32000	00130	Advance storage address
00104	45	00000	00074	
00105	21	00115	00111	Advance storage address
00106	45	00000	00013	
00107	16	00133	00115	Enter IA to transfer instruction
00110	45	00000	00013	
00111	00	00000	01500	Maximum buffer size
00112	11	00133	00300	First transfer
00113	00	00000	00077	Data mask
00114	00	00000	00000	Seventh level code
00115	00	00000	00000	Insert address
00116	00	00000	17700	Seventh level mask
00117	00	00000	10100	ED code
00120	00	00000	11100	IA code
00121	00	00000	10500	CA code
00122	00	00000	00300	Stop code
00123	00	00000	00274	Check-sum check address
00124	00	00000	00001	Constant
00125	11	00133	02000	Last transfer
00126	75	30000	00077	Transfer instruction
00127	00	00000	02000	Threshold constant

TABLE 2. FRI-2 LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00130	00	00000	00000	MC insert address constant
00131	00	00000	00000	Computed CS
00132	00	00000	00000	
00133	00	00000	00000	Word assembly
00134	16	32000	00001	Store Beginning address (v)
00135	11	00204	31000	Isolate number of transfers (Mk)
00136	51	00075	32000	
00137	32	00002	00071	Determine number of words to be punched.
00140	55	00001	00017	
00141	35	31000	31000	Enter punch parameters
00142	56	10000	00143	Stop before punching
00143	37	00264	00213	Jump to punch sub-routine
00144	15	00210	00162	Restore conditional program modification instructions.
00145	15	00266	00160	
00146	16	00205	00126	
00147	27	00001	00001	Clear CS cells
00150	27	00002	00002	
00151	45	20000	00153	Optional punch CS
00152	45	00000	00077	
00153	11	00131	00272	Enter computed CS
00154	11	00132	00273	
00155	11	00200	31000	Enter CS punch parameters and punch
00156	37	00264	00213	
00157	45	00000	00077	Return to read mode

TABLE 2. FRI-2 LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00160	16	00201	00126	Modify program when buffer is not full
00161	45	00000	00031	
00162	16	00202	00126	Modify program when buffer is full
00163	45	00000	00066	
00164	00	00001	00000	Constant
00165	16	32000	00001	Store beginning address
00166	11	00204	31000	Isolate and store number of transfers
00167	51	00075	32000	
00170	35	00002	00002	
00171	15	00265	00160	Conditional program modification
00172	15	00207	00162	
00173	45	00000	00077	
00174	00	00000	00160	Constants
00175	00	00000	00162	
00176	00	00000	00031	
00177	00	00000	00066	
00200	00	00272	00002	
00201	00	00000	00134	
00202	00	00000	00165	
00203	00	00000	00135	
00204	00	07777	00000	
00205	00	00000	00077	
00206	00	00000	00166	
00207	00	00206	00000	
00210	00	00202	00000	

TABLE 2. FRI-2 LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00211	00	00000	00000	
00212	00	00000	00000	
00213	15	31000	00211	
00214	16	31000	00212	
00215	45	30000	00144	
00216	23	30000	30000	
00217	75	00020	00221	
00220	63	00000	31000	
00221	63	10000	31000	
00222	63	00000	31000	
00223	63	00000	31000	
00224	63	10000	31000	Punch storage for reload
00225	31	00211	00055	
00226	63	00000	32000	
00227	54	32000	00006	
00230	63	00000	32000	
00231	54	32000	00006	
00232	63	10000	32000	
00233	11	00211	31000	
00234	45	00000	00253	
00235	15	31000	00236	
00236	31	00000	00052	
00237	63	00000	32000	
00240	54	32000	00006	
00241	63	00000	32000	

TABLE 2. FRI-2 LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00242	54	32000	00006	Punch storage for reload (cont.)
00243	63	00000	32000	
00244	54	32000	00006	
00245	63	00000	32000	
00246	54	32000	00006	
00247	63	00000	32000	
00250	54	32000	00006	
00251	63	10000	32000	
00252	21	31000	00164	
00253	41	00212	00235	
00254	75	00003	00256	
00255	63	00000	31000	
00256	31	31000	00055	
00257	63	10000	32000	
00260	54	32000	00006	
00261	63	00000	32000	
00262	54	32000	00006	
00263	63	10000	32000	
00264	45	00000	00000	
00265	00	00203	00000	Constants
00266	00	00201	00000	
00267	16	00006	00110	Clear CS cells after punching and by-pass CS test.
00270	27	00123	00123	
00271	45	10000	00007	

TABLE 2. FRI-2 LOADING ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00272		CS		A_L
00273		CS		A_R

MAINTENANCE ROUTINES

MAGNETIC DRUM TEST

1. GENERAL

This program performs 132 tests. These tests check the ability of the Magnetic Drum Storage System to read or write information correctly in every cell on the drum. In general, each test executes a different basic transfer instruction (BTI) which, when repeated, transfers a pattern of words from consecutive drum addresses, starting at a particular u address (BTI_u), to consecutive drum addresses, starting at a particular v address (BTI_v). The transmitted pattern is then checked against the original pattern to detect whether or not an error has occurred.

Four types of basic transfer instructions are used. The first 32 BTI's, the write transient transfers, test the ability of the system to transmit information correctly from a set of drum addresses to another set in the same MD group. The next 96 BTI's, the group switch transfers, test the ability of the system to transmit information from one MD group to another. The next two BTI's, the write lockout transfers, check the lockout feature, which prevents reading from occurring too soon after writing. The last two BTI's, the group switch lockout transfers, check the lockout feature which prevents the reading from occurring before the MD GS I and GS II flip-flops have had time to switch the MD group enables to the proper voltage levels.

When the program starts, a pattern of 512 words is developed in the rapid-access storage. Next, a transfer test cycle, performed a maximum of 128 times, tests the system using the 32 write transient transfers and the 96 group switch transfers. If an error occurs during any of these tests, an error print-out routine causes the typewriter to print a sentence that identifies the error. If 128 transfer tests are performed and no errors have been detected, the two write lockout tests are performed next. If no error occurs, the two group lockout tests are performed next. If an error occurs during one of the write lockout or group lockout tests, the typewriter prints a sentence that identifies the type of error that occurred.

2. PROCEDURE

The MD test is contained on the master test tape and is normally loaded onto the drum in preparation for the maintenance runs. If, however, the maintenance routines are not on the drum, and it is desired to run the MD test, the special tape containing the MD test only may be loaded on the drum, starting at address 47000.

To run the test, perform the following operations.

Step 1. Insert paper into the typewriter carriage and set the typewriter power switch to the ON position.

Step 2. At the Supervisory Control Panel, set the TEST SWITCH GROUP MD AMPLIFIER MARGINAL CHECK switch to the "up" position. If the test is to be executed on high margin, set the TEST SWITCH GROUP HI - LO switch to the HI position, or if the test is to be executed at low margin, set this switch to the LO position.

Step 3. Set PAK to 47000
Optional selections described below
OPERATING GROUP---START

Optional selections are listed below. The STOP selections may be made at any time. The JUMP selections may be made or dropped only when the computer is stopped.

Select these as follows:

(1) SELECTIVE STOPS GROUP - SELECT STOP 3 to stop after a test error occurs. (After an error, the entire test is restarted.)

(2) SELECTIVE STOPS GROUP - SELECT STOP 2 to stop at end of test.

(3) SELECTIVE JUMPS GROUP - SELECT JUMP 2 to cause an entire test to be repeated. (If not selected, a Final Stop will occur.)

3. THEORY OF THE TEST

Instructions 47000 through 47007 transfer the test and the Type Text subroutine from the drum to rapid-access storage. After this has been done, the test routine and the subroutine are executed solely in the rapid-access storage, beginning with address 00033. Instruction 00033 inserts a starting and resume address into Q for use during the Type Text subroutine 00400 through 00430. Next, 00034 produces a jump to the Type Text subroutine. The contents of 00036 through 00041, "MD STORAGE TEST", are typed.

Instructions 00042 through 00044 generate a pattern of 512 words. Each word of this pattern consists of 35 zeros and a single one. In any 36 consecutive words of this pattern each word has the single one bit in a different binary position. After the pattern has been developed, a jump is executed to the transfer tests which start at 00045.

a. TRANSFER TESTS. - (See Figure 1.) The transfer tests are performed by a main indexed cycle performed 128 times, and an indexed subcycle performed twice during each of the main cycles. Each main cycle performs one transfer test which uses one of the first 128 BTI's. If no errors occur during any of the 128 tests, the transfer test cycle is repeated until all the 128 transfer tests BTI's have been used. However, if an error occurs during any transfer test, a jump is made to an error print-out operation which starts at 00156. This operation prints the number of the failed digits and prints addresses which identify the BTI which caused the test to fail. When this operation has been completed, the equipment stops.

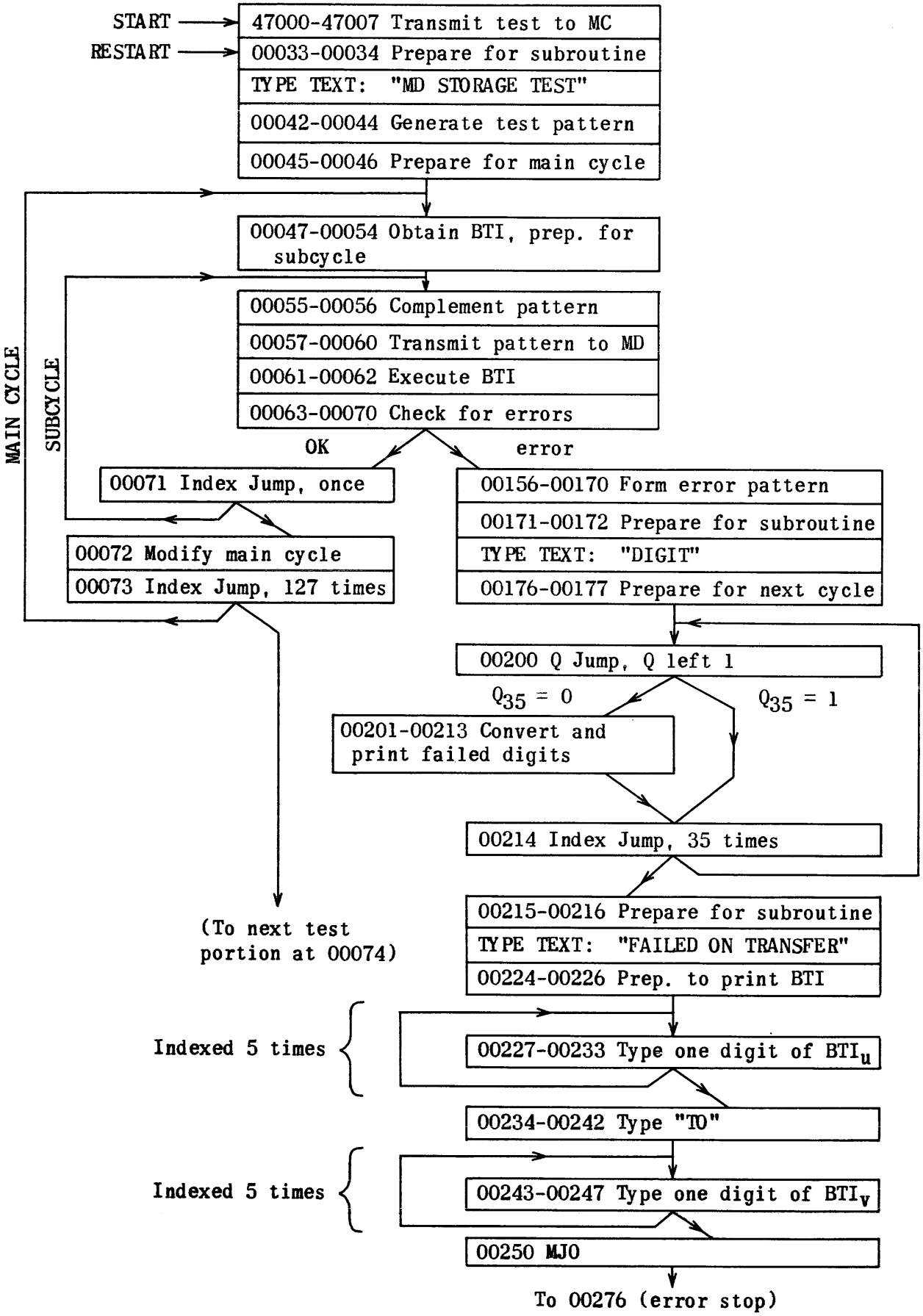


Figure 1. Transfer Test Portion of MD Test
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At the start of the transfer test, instructions 00045 and 00046 modify the cycle so that the first cycle is performed with the proper BTI. Instructions 00047-00053 transmit the first BTI into 00062, transmit the u-address portion of BTI (BTI_u) into 00067, and transmit the v-address portion of BTI (BTI_v) into 00060. Instruction 00054 sets index 00027 to 1. This is done so that the subcycle consisting of instructions 00055 through 00071 will be performed twice. During each main transfer test cycle, the first performance of this subcycle tests the drum system, using the complement of the original pattern, and the second performance tests the drum system with the original test pattern.

During each of the two subcycle performances, instructions 00055 and 00056 complement the test pattern in MC. Instructions 00057 and 00060 transmit the complemented pattern into the drum at starting address BTI_u. Next, 00061 and 00062 execute the current basic transfer instruction, BTI. Repeated performances of this instruction transmit the complemented pattern to another section of the drum at starting address BTI_v.

During each subcycle, instructions 00063 through 00070 check the presence of errors. The sum of all 36 words of the MC pattern is formed in A. The sum of the pattern in the drum section BTI_v is subtracted from A. If an error has occurred, A is not zero and a jump is made to the error print-out operation at 00156. If no error has occurred, A is equal to zero and a jump is made to Index Jump instruction 00071, which causes the subcycle starting at 00055 to be repeated once during each transient test. The repeat performance of this subcycle recomplements the pattern so that the test is performed with the original pattern.

If the subcycle has been performed twice and no error has occurred, 00072 increases the u address portion of 00047 by one count, and 00073 executes a jump to 00047, so that the next transfer test cycle is performed with a new BTI. After 128 cycles have been executed, 00073 is followed by the next tests, at 00074.

If an error occurs during any of the test subcycles, 00070 produces a jump to the error print-out routine at 00156. The purpose of this routine is to type out a sentence that identifies the error. For example, the failure of digit 34 during the test using the first BTI is identified by a typed sentence as follows: "DIGIT 34 FAILED ON TRANSFER 40000 to 46000."

In the error print-out routine, instruction 00156 inserts the address BTI_v into instruction 00160, and repeated instruction 00160 forms the bit-by-bit sums of the pattern word from MC and the drum pattern words which start at address BTI_v. If no errors are present, the resulting "error words" in MC are all equal to zero. If errors occur, "1" bits are present where a bit has failed to transfer properly. The resulting 512 error words in MC are complemented so that "0" bits are formed in erroneous digit positions and "1" bits are formed in the other positions. A composite error word is formed by 00163, 00164, and 00165. These instructions form the bit-by-bit product of the 512 error words in Q, and the resulting error word contains "0" bits in every digit failure position. Next, 00171 and 00172 introduce the type text subroutine which types "DIGIT". Instruction 00176 transmits the error word to Q, and 00177 sets an index for use in the next cycle.

The composite error word is examined for the presence of "0" bits, and the positions of each "0" bit are typed in decimal notation. This is accomplished by 36 performances of an indexed cycle starting at 00200. During each cycle, 00200 is followed by a decimal conversion operation at 00201 if the left-hand bit of Q is equal to "0", or is followed by Index Jump instruction 00214 if the left-hand bit of Q is "1". In either case, Q is shifted left by one place. Each time a "0" bit is detected the decimal conversion routine causes the typewriter to print a digit number from 0 to 35. After 36 cycles, all the faulty digits have been identified and the next instruction is 00215.

Instructions 00215 and 00216 introduce the Type Text subroutine, which at this time prints "FAILED ON TRANSFER".

Next, the last-used BTI is shifted in Q, so that the address BTI_u is in the left-hand end of A_L. An indexed cycle 00227 through 00233, performed five times, prints the five octal digits of BTI_u. Instructions 00234 through 00241 type the word "TO". The index used in the last cycle is reset to 4 by 00242, and the program proceeds to 00243.

Another indexed cycle 00243 through 00247, also performed five times, types the five octal digits of BTI_v. After this is done, the typewriter will have completed the sentence "DIGIT - FAILED ON TRANSFER -----TO-----". A jump to 00276 is executed. If MS3 has been selected, the equipment stops on 00277. If MS3 is not selected, 00277 produces a jump to 00033 so that the transfer tests are repeated.

b. WRITE LOCKOUT TESTS. - (See Figure 2.) When instruction 00073 is executed the 128th time, it is followed by 00074, and the write lockout tests start. Instruction 00074 sets a test cycle index 00021 to one, 00075 inserts the address of the 129th BTI into 00076, and then an indexed cycle starts at 00076.

The write lockout tests are accomplished by a main indexed cycle performed twice: once with the 129th BTI and once with the 130th BTI. A subcycle is performed twice during each main cycle: once with the original test pattern and once with the complemented test pattern.

During each performance of the indexed cycle, 00076 transmits the BTI into 00111, 00077 and 00100 transmit the address BTI_v into the u-address portion of 00116, and 00101 and 00102 the address BTI_u into the v-address portion of 00107.

The subcycle 00104 through 00117, performed twice during each test cycle, complements 64 words of the rapid-access pattern, transmits these words to consecutive drum addresses starting at BTI_u, executes the BTI (stored in 00111) by repeatedly transmitting the pattern from starting address BTI_u to starting address BTI_v, then performs a check for errors. During the check, 00112 clears AR, 00113 and 00114 form the sum of the MC pattern in A, and 00115 and 00116 subtract the sum of the BTI_v pattern from A. If no errors occur, A becomes equal to zero, and Zero Jump 00117 is followed by Index Jump 00120, which causes the subcycle to be repeated. During the second subcycle, the complemented test pattern is recomplemented by 00104 and 00105, so that the original test pattern is restored and used with the current BTI.

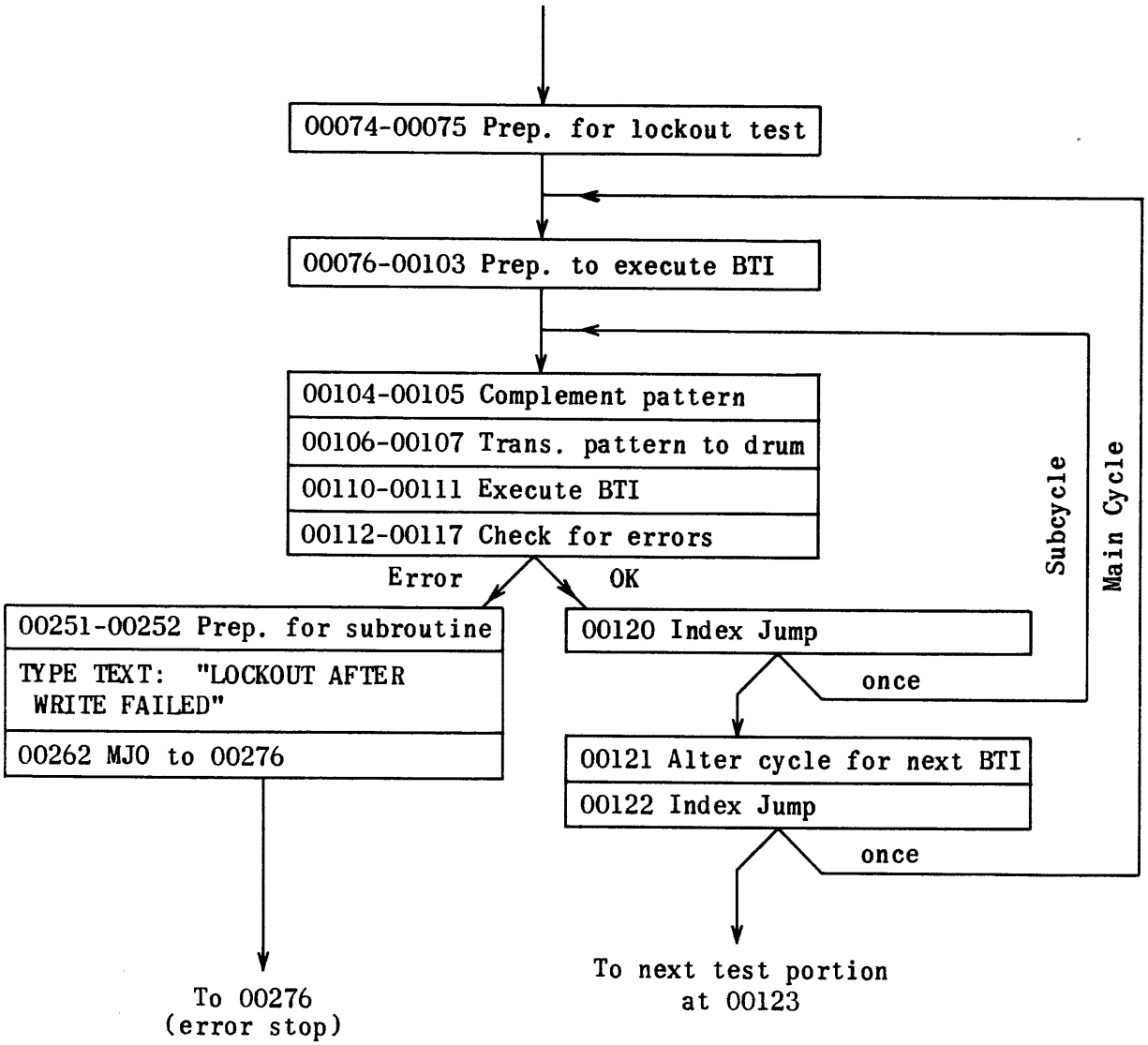

Figure 2. Write Lockout Portion of MD Test
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If an error occurs during either cycle, 00117 finds that A is not zero and a jump to 00251 is executed. Instructions 00251 and 00252 introduce the Type Text subroutine which types "LOCKOUT AFTER WRITE FAILED". After this is done, 00262 produces a jump to 00276 and 00277, which causes the program to stop if MS3 has been selected. Instruction 00277 produces a jump to restart the entire test program when operation is resumed.

If no error occurs, the second performance of the test subcycle 00104 through 00120 is followed by 00121. Instruction 00121 advances the u address of 00076, so that, during the test, the next BTI (BTI 130) is used. If only one BTI has been used for a write lockout test, 00122 executes a jump to 00076 and the test is repeated. If both BTI 129 and BTI 130 have been used, 00122 is followed by 00123, and the group switch lockout tests are started.

c. GROUP SWITCH LOCKOUT TESTS. - (See Figure 3.) The group switch lockout tests are accomplished by an indexed cycle performed twice: once with BTI 131 and once with BTI 132. A subcycle is performed twice during each main cycle: once with the original test pattern and once with the complemented test pattern. Before the main cycle starts, 00123 resets index 00021 to one, and 00124 inserts the address of BTI 131 into 00125.

During each performance of the main cycle, which starts at 00125, 00125 transmits the BTI into 00143, 00126 and 00127 transmit the address BTI_u into the v-address portion of 00135, 00130 transmits BTI_v into the v portion of 00141, and 00131 transmits BTI_u into the u portion of 00150. Instruction 00132 resets an index value for the subcycle.

The subcycle 00133 through 00151, performed twice during each test cycle, forms 64 consecutive zero words in the drum, starting at address BTI_u, writes the complement of a 64-word test pattern from rapid-access storage to the drum starting at address BTI_v, and executes the BTI by forming 64 words in the drum starting at address BTI_u. Each word formed by the BTI is the sum of a zero word and one of the complemented test pattern words. A check for errors is performed by 00144 through 00151. A_R is cleared, the original (complemented) test pattern is added to A, and the list of sums starting at BTI_u is subtracted from A. If no errors occur, (A) becomes equal to zero, and 00151 is followed by Index Jump 00152 which causes the subcycle to be repeated once. During the second subcycle, the test pattern is recomplemented.

If an error occurs, 00151 produces a jump to 00263 and 00264, which prepares the Type Text Subroutine for typing "LOCKOUT AFTER GROUP SWITCH FAILED". After the Type Text subroutine is completed, 00262 executes a jump to 00276 and 00277, to stop the program if MS3 has been selected. A restart after 00277 causes the entire MD Test Routine to be restarted.

If no error occurs, the second performance of the subcycle is followed by 00153, which advances the u-address portion of 00125, so that the next test is performed with the last BTI. When the last BTI has been used and no errors have occurred, 00154 is followed by 00155 which executes a jump to 00300. Instructions 00300 and 00301 prepare the Type Text subroutine. This time "OK" is typed to indicate that the entire test of 132 BTI's has been performed without error. After this is done, 00304 resets F_1 to the proper jump address for

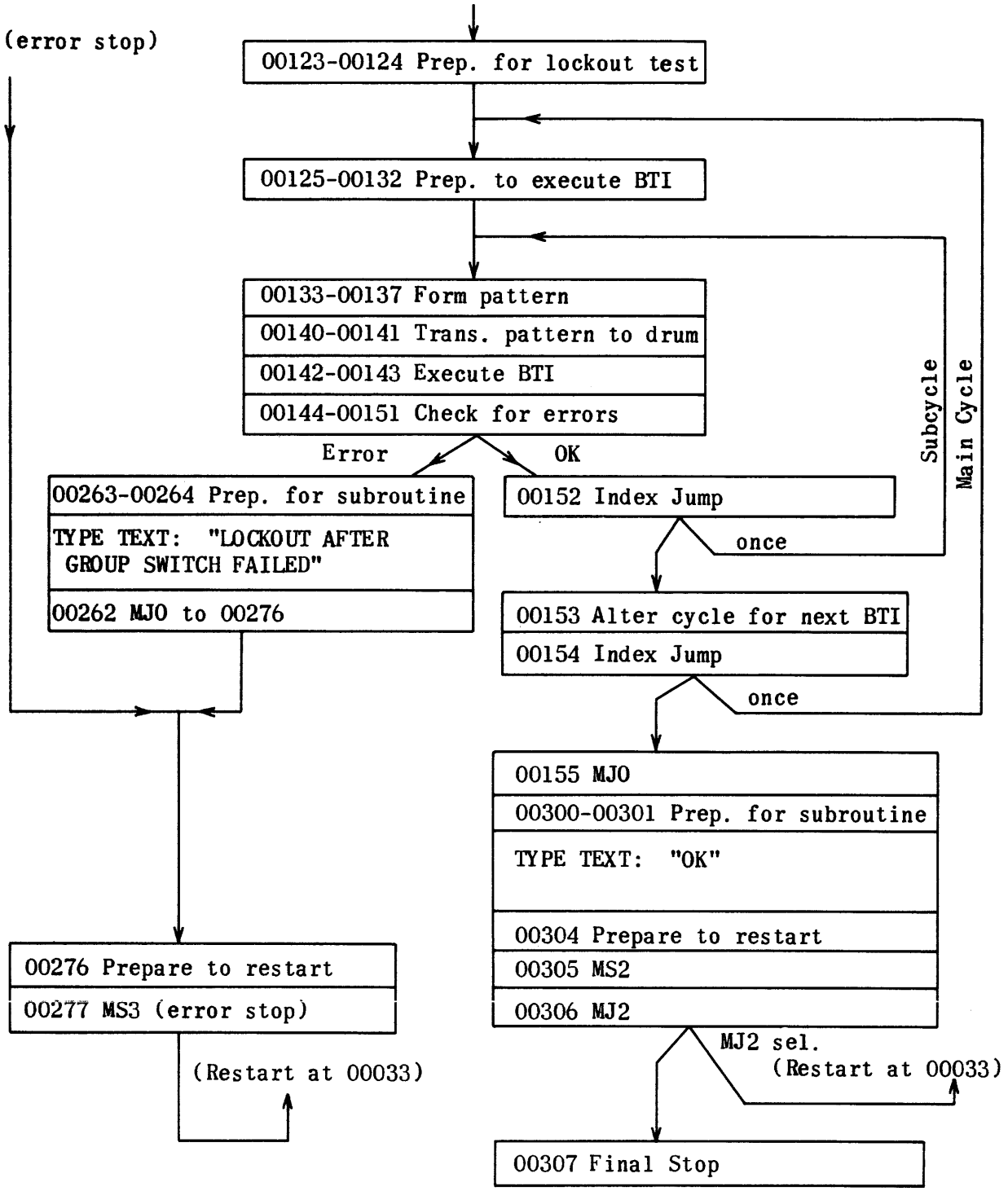

Figure 3. Group Switch Lockout Portion of MD Test
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restarting, and 00305 executes a stop if MS2 is selected. This is followed by 00306, which either executes a jump to restart the entire test routine if MJ2 is selected or to Final Stop instruction 00307 if MJ2 is not selected.

TABLE 1. MD TEST ROUTINE

PROGRAM: MD Storage Test

DESCRIPTION: Test all storage positions on the magnetic drum. Test the read lockout after writing and group switching. Select MS3 to stop after an error. Select MJ2 to repeat test. Select MS2 to stop at end of test.

ADDRESS	OP-CODE	u	v	FUNCTION
				Transfer Test and Subroutine to MC
47000	11	47001	00000	Enter jump instruction in F_1
47001	45	00000	47002	Jump to 47002
47002	75	30031	47004	Transfer type text subroutine to MC
47003	11	47524	00400	
47004	75	30204	47006	Transfer test to MC
47005	11	47010	00440	
47006	75	30310	00033	
47007	11	47214	00000	
47010 thru 47213				See 00440 thru 00643 below
47214 thru 47523				See 00000 thru 00307 below
47524 thru 47555				Type Text Subroutine
00000	45	00000	00033	Jump to start
00001	00	00000	00037	0
00002	00	00000	00011	1
00003	00	00000	00074	2
00004	00	00000	00070	3
00005	00	00000	00064	4
00006	00	00000	00062	5
00007	00	00000	00066	6

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00010	00	00000	00072	7
00011	00	00000	00060	8
00012	00	00000	00033	9
00013	00	00000	00004	Constant
00014	--	-----	-----	Index counter
00015	00	00000	00012	Constant (decimal 10)
00016	00	00000	00043	Constant (decimal 35)
00017	--	-----	-----	Index counter
00020	00	00000	00177	Constant
00021	--	-----	-----	Index counter
00022	00	00000	00007	Mask
00023	--	-----	-----	Temporary storage
00024	00	00001	00000	Constant
00025	00	00440	00000	Constant
00026	00	00000	00001	Constant
00027	--	-----	-----	Index counter
00030	61	00000	00001	Constant
00031	00	00640	00000	Constant
00032	00	00642	00000	Constant
				Type Heading
00033	11	00035	31000	Enter type parameters in Q
00034	45	00000	00400	Jump to subroutine
00035	00	00036	00042	Type parameters

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	●	▼	FUNCTION
00036	45	45470	72204	cr cr up M D sp
00037	24	01031	23013	S T O R A G
00040	20	04012	02401	E sp T E S T
00041	04	57575	75757	sp dn dn dn dn dn
00042	11	00026	20000	Enter +1 in A
00043	75	11000	00045	Generate 512 word test pattern
00044	35	32000	01000	
				Digit Test
00045	11	00020	00021	Set index counter
00046	15	00025	00047	Insert address of first transfer instruction
00047	11	-----	00062	Enter transfer instruction in 00062
00050	31	00062	00017	Modify instruction at 00067
00051	15	32000	00067	
00052	54	32000	00052	Modify instruction at 00060
00053	16	32000	00060	
				Basic Step I
00054	11	00026	00027	Set index counter
00055	75	31000	00057	Complement pattern
00056	13	01000	01000	
00057	75	31000	00061	Transfer pattern to M D
00060	11	01000	-----	
00061	75	31000	00063	Transfer pattern within M D
00062	--	-----	-----	

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				Verify I
00063	23	32000	32000	Clear A
00064	75	21000	00066	Split add pattern words in MC
00065	32	01000	00000	
00066	75	21000	00070	Split subtract pattern words in MD
00067	34	-----	00000	
00070	47	00156	00071	Zero jump
				Index I
00071	41	00027	00055	Index jump - 1 time
00072	21	00047	00024	Advance address
00073	41	00021	00047	Index jump - 127 times
				Test Lockout after write
00074	11	00026	00021	Set index counter
00075	15	00031	00076	Insert address of first test instruction
00076	11	-----	00111	Enter test instruction in 00111
00077	31	00111	00017	Modify instruction at 00116
00100	15	32000	00116	
00101	54	32000	00052	Modify instruction at 00107
00102	16	32000	00107	
00103	11	00026	00027	Set index counter
00104	75	30100	00106	Complement pattern
00105	13	01000	01000	

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	α	ν	FUNCTION
00106	75	30100	00110	Transfer pattern to MD
00107	11	01000	-----	
00110	75	30100	00112	Transfer pattern within MD
00111	--	-----	-----	
				Verify II
00112	23	32000	32000	Clear A
00113	75	20100	00115	Split add pattern words in MC
00114	32	01000	00000	
00115	75	20100	00117	Split subtract pattern words in MD
00116	34	-----	00000	
00117	47	00251	00120	Zero jump
				Index II
00120	41	00027	00104	Index jump -1 time
00121	21	00076	00024	Advance address
00122	41	00021	00076	Index jump -1 time
				Test Lockout After Group Switch
00123	11	00026	00021	Set index counter
00124	15	00032	00125	Insert address of first test instruction
00125	11	-----	00143	Enter test instruction in 00143
00126	31	00143	00071	Modify instructions at 00141 and 00150
00127	16	32000	00135	
00130	16	00143	00141	
00131	15	00143	00150	

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	●	▼	FUNCTION
				Basic Step III
00132	11	00026	00027	Set index counter
00133	23	32000	32000	Clear A
00134	75	10100	00136	Clear block of 64 MD addresses
00135	11	32000	-----	
00136	75	30100	00140	Complement pattern
00137	13	01000	01000	
00140	75	30100	00142	Transfer pattern to MD
00141	11	01000	-----	
00142	75	30100	00144	Perform test in MD
00143	--	-----	-----	
				Verify III
00144	23	32000	32000	Clear A
00145	75	20100	00147	Split add pattern words in MC
00146	32	01000	00000	
00147	75	20100	00151	Split subtract pattern words in MD
00150	34	-----	00000	
00151	47	00263	00152	Zero jump
				Index III
00152	41	00027	00133	Index jump -1 time
00153	21	00125	00024	Advance address
00154	41	00021	00125	Index jump -1 time
00155	45	00000	00300	Jump to type "OK"

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	a	v	FUNCTION
				Generate Error Pattern
00156	16	00062	00160	Enter MD address in 00160
00157	75	31000	00161	Form error pattern
00160	27	01000	-----	
00161	75	31000	00163	Complement error pattern
00162	13	01000	01000	
00163	11	01000	31000	Enter error digits as 0's in Q
00164	75	20777	00166	
00165	51	01001	31000	
00166	75	31000	00170	Restore error pattern
00167	13	01000	01000	
				Type Failing Digits
00170	11	31000	00023	Store failing digits
00171	11	00173	31000	Enter type parameters in Q
00172	45	00000	00400	Jump to subroutine
00173	00	00174	00176	Type parameters
00174	47	45040	42214	up cr sp sp D I
00175	13	14010	40457	G I T sp sp dn
00176	11	00023	31000	Enter failing digits in Q
00177	11	00016	00017	Set index counter
00200	44	00214	00201	Q jump
00201	11	31000	00023	Store failing digits
00202	11	00017	32000	Enter digit number in A

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	a	v	FUNCTION
00203	73	00015	31000	Octal to decimal conversion
00204	35	00030	00210	
00205	11	32000	32000	
00206	35	00030	00207	
00207	--	-----	-----	Type digit number
00210	--	-----	-----	
00211	61	00000	00013	Two spaces
00212	61	00000	00013	
00213	11	00023	31000	Enter failing digits in Q
00214	41	00017	00200	Index jump - 35 times
				Type "Failed on Transfer"
00215	11	00217	31000	Enter type parameters in Q
00216	45	00000	00400	Jump to subroutine
00217	00	00220	00224	Type parameters
00220	45	47040	42630	cr up sp sp F A
00221	14	11202	20403	I L E D sp 0
00222	06	04011	23006	N sp T R A N
00223	24	26201	20457	S F E R sp dn
00224	11	00013	00014	Set index counter
00225	11	00062	31047	Enter transfer instruction in Q
00226	55	31000	00006	Shift Q 6 places
00227	55	31000	00003	Convert address digit
00230	51	00022	31001	
00231	35	00030	00232	

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	α	ν	FUNCTION
00232	--	-----	-----	Type address digit
00233	41	00014	00227	Index jump - 4 times
00234	61	00000	00013	Space
00235	61	00000	00225	Shift up
00236	61	00000	00230	Type "T"
00237	61	00000	00221	Type "0"
00240	61	00000	00223	Shift down
00241	61	00000	00013	Space
00242	11	00013	00014	Set index counter
00243	55	31000	00003	Convert address digit
00244	51	00022	32000	
00245	35	00030	00246	
00246	--	-----	-----	Type address digit
00247	41	00014	00243	Index jump - 4 times
00250	45	00000	00276	Jump to error stop
				Type "Write Lockout Failed"
00251	11	00253	31000	Enter type parameters in Q
00252	45	00000	00400	Jump to sub routine
00253	00	00254	00262	Type parameters
00254	47	45040	41103	up cr sp sp L 0
00255	16	36033	40104	C K O U T sp
00256	30	26012	01204	A F T E R sp
00257	31	12140	12004	W R I T E sp

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00260	26	30141	12022	F A I L E D
00261	04	04575	75757	sp sp dn dn dn dn
00262	45	00000	00276	Jump to error stop
				Type "Group Switch Lockout Failed"
00263	11	00265	31000	Enter type parameters in Q
00264	45	00000	00400	Jump to subroutine
00265	00	00266	00275	Type parameters
00266	47	45040	31103	up cr sp sp L O
00267	16	36033	40104	C K O U T sp
00270	30	26012	01204	A F T E R sp
00271	13	12033	41504	G R O U P sp
00272	24	31140	11605	S W I T C H
00273	04	26301	41120	sp F A I L E
00274	22	04045	75757	D sp sp dn dn dn
00275	45	00000	00276	Jump to error stop
				Error Stop
00276	16	00012	00000	Restore jump to start
00277	56	30000	00000	MS 3
				Type "OK"
00300	11	00302	31000	Enter type parameters in Q
00301	45	00000	00400	Jump to subroutine
00302	00	00303	00304	Type parameters

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00303	47	03365	75757	up 0 K dn dn dn
				Conclude Test
00304	16	00012	00000	Restore jump to start
00305	56	20000	00306	MS 2
00306	45	20000	00000	MJ 2
00307	57	-----	-----	Stop
				Basic Transfer Instructions for Write Transient Test
00440	11	40000	46000	BTI 1
00441	11	41000	47000	BTI 2
00442	11	42000	40001	BTI 3
00443	11	43000	41001	BTI 4
00444	11	44000	42001	BTI 5
00445	11	45000	43001	BTI 6
00446	11	46000	44001	BTI 7
00447	11	47000	45001	BTI 8
00450	11	50000	56000	BTI 9
00451	11	51000	57000	BTI 10
00452	11	52000	50001	BTI 11
00453	11	53000	51001	BTI 12
00454	11	54000	52001	BTI 13
00455	11	55000	53001	BTI 14
00456	11	56000	54001	BTI 15

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00457	11	57000	55001	BTI 16
00460	11	60000	66000	BTI 17
00461	11	61000	67000	BTI 18
00462	11	62000	60001	BTI 19
00463	11	63000	61001	BTI 20
00464	11	64000	62001	BTI 21
00465	11	65000	63001	BTI 22
00466	11	66000	64001	BTI 23
00467	11	67000	65001	BTI 24
00470	11	70000	76000	BTI 25
00471	11	71000	77000	BTI 26
00472	11	72000	70001	BTI 27
00473	11	73000	71001	BTI 28
00474	11	74000	72001	BTI 29
00475	11	75000	73001	BTI 30
00476	11	76000	74001	BTI 31
00477	11	77000	75001	BTI 32
				Basic Transfer Instructions for Group Switch Test
00500	11	40000	56000	BTI 33
00501	11	41000	57000	BTI 34
00502	11	42000	50001	BTI 35
00503	11	43000	51001	BTI 36

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00504	11	44000	52001	BTI 37
00505	11	45000	53001	BTI 38
00506	11	46000	54001	BTI 39
00507	11	47000	55001	BTI 40
00510	11	40000	66000	BTI 41
00511	11	41000	67000	BTI 42
00512	11	42000	60001	BTI 43
00513	11	43000	61001	BTI 44
00514	11	44000	62001	BTI 45
00515	11	45000	63001	BTI 46
00516	11	46000	64001	BTI 47
00517	11	47000	65001	BTI 48
00520	11	40000	76000	BTI 49
00521	11	41000	77000	BTI 50
00522	11	42000	70001	BTI 51
00523	11	43000	71001	BTI 52
00524	11	44000	72001	BTI 53
00525	11	45000	73001	BTI 54
00526	11	46000	74001	BTI 55
00527	11	47000	75001	BTI 56
00530	11	50000	46000	BTI 57
00531	11	51000	47000	BTI 58
00532	11	52000	40001	BTI 59
00533	11	53000	41001	BTI 60

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00534	11	54000	42001	BTI 61
00535	11	55000	43001	BTI 62
00536	11	56000	44001	BTI 63
00537	11	57000	45001	BTI 64
00540	11	50000	66000	BTI 65
00541	11	51000	67000	BTI 66
00542	11	52000	60001	BTI 67
00543	11	53000	61001	BTI 68
00544	11	54000	62001	BTI 69
00545	11	55000	63001	BTI 70
00546	11	56000	64001	BTI 71
00547	11	57000	65001	BTI 72
00550	11	50000	76000	BTI 73
00551	11	51000	77000	BTI 74
00552	11	52000	70001	BTI 75
00553	11	53000	71001	BTI 76
00554	11	54000	72001	BTI 77
00555	11	55000	73001	BTI 78
00556	11	56000	74001	BTI 79
00557	11	57000	75001	BTI 80
00560	11	60000	46000	BTI 81
00561	11	61000	47000	BTI 82
00562	11	62000	40001	BTI 83
00563	11	63000	41001	BTI 84

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00564	11	64000	42001	BTI 85
00565	11	65000	43001	BTI 86
00566	11	66000	44001	BTI 87
00567	11	67000	45001	BTI 88
00570	11	60000	56000	BTI 89
00571	11	61000	57000	BTI 90
00572	11	62000	50001	BTI 91
00573	11	63000	51001	BTI 92
00574	11	64000	52001	BTI 93
00575	11	65000	53001	BTI 94
00576	11	66000	54001	BTI 95
00577	11	67000	55001	BTI 96
00600	11	60000	76000	BTI 97
00601	11	61000	77000	BTI 98
00602	11	62000	70001	BTI 99
00603	11	63000	71001	BTI 100
00604	11	64000	72001	BTI 101
00605	11	65000	73001	BTI 102
00606	11	66000	74001	BTI 103
00607	11	67000	75001	BTI 104
00610	11	70000	46000	BTI 105
00611	11	71000	47000	BTI 106
00612	11	72000	40001	BTI 107

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00613	11	73000	41001	BTI 108
00614	11	74000	42001	BTI 109
00615	11	75000	43001	BTI 110
00616	11	76000	44001	BTI 111
00617	11	77000	45001	BTI 112
00620	11	70000	56000	BTI 113
00621	11	71000	57000	BTI 114
00622	11	72000	50001	BTI 115
00623	11	73000	51001	BTI 116
00624	11	74000	52001	BTI 117
00625	11	75000	53001	BTI 118
00626	11	76000	54001	BTI 119
00627	11	77000	55001	BTI 120
00630	11	70000	66000	BTI 121
00631	11	71000	67000	BTI 122
00632	11	72000	60001	BTI 123
00633	11	73000	61001	BTI 124
00634	11	74000	62001	BTI 125
00635	11	75000	63001	BTI 126
00636	11	76000	64001	BTI 127
00637	11	77000	65001	BTI 128

TABLE 1. MD TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				Basic Transfer Instructions For Write Lockout Test
00640	11	50000	57400	BTI 129
00641	11	50000	56400	BTI 130
				Basic Transfer Instructions For Group Switch Test
00642	21	50000	61000	BTI 131
00643	21	50000	62000	BTI 132

MAGNETIC CORE STORAGE TEST

1. GENERAL

The magnetic core storage test program is performed to check the ability of the MCS System to correctly read, write, restore, and hold information. Eleven tests are combined in one test program. Test A is the hold/restore "1's" test, and checks the ability of each bit of each MC address to hold and restore a "1". (Test a1 is the hold "1's" test, and test a2 is the restore "1's" test.) Test B is the hold/restore "0's" test and checks the ability of each bit of each MC address to hold and restore a "0". (Test b1 is the hold "0's" test, and test b2 is the restore "0's" test.) Test C is the MC Address Register test, and checks the ability of each flip-flop of the MC Address Register to switch to the "0" or "1" state at high speed. Test D is the hold-worst pattern test, and checks the ability of the MCS system to hold information under the worst signal/noise ratio condition. Test E is the hold complement worst pattern test, and checks the ability of the MCS system to hold information under the complement worst signal/noise ratio condition. Test F is the circulate worst pattern test, and is similar to test D, but the entire pattern is circulated backward one address at a time. Test F, therefore, checks the same transmission paths as Test D but under varying signal to noise ratio conditions. Test G is the crosstalk test, and is similar to test D, but it also checks for crosstalk between bits. Test H is also a crosstalk test, and is similar to test G, except that it checks the MC addresses for crosstalk that are not checked by Test G. Test I is the disturb sensitivity test, and checks the ability of each magnetic core of the MCS system to hold a "1" in the presence of repeated inhibit pulses. Test J is another worst pattern test, but the program of instructions for this test is stored in the MCS system, because it would take too long to perform this test using the worst pattern with a program which is stored in MD. In Test J the contents of each MC address are complemented and then checked to determine whether they can be correctly read. Test J uses a program of instructions which is first stored in MCS addresses 00000 through 00025, and another similar program is stored in MCS addresses 07754 through 07777. (Test j1 uses the worst pattern, and test j2 uses the complement worst pattern.) Test K is a test of the logical circuits connected with the partial write instructions 15 and 16. It tests the operation of the partial write flip-flops V21-071 and V21-061 and their gates V07-061, V03-071, V05-061, and V07-071. Test k1 tests the 15 instruction, and test k2 tests the 16 instruction.

If the MC Storage Test is to be run as the Short MC Storage Test, MJ3 is selected before the test is begun. When the Short MC Storage Test is run, tests a2, b2, F, and K are bypassed, and the error search subroutine is bypassed. The regular MC Storage Test takes 4 minutes to run. The Short MC Test takes 40 seconds to run.

2. PROCEDURE

The MC test routine is loaded from punched paper tape, or magnetic tape, into the magnetic drum starting at address 40000 (see Table 3).

To run the test, use the following procedure:

Step 1. Insert paper in the typewriter, and set the typewriter power switch to the ON position.

Step 2. Optional selections are listed below. The STOP selections may be made at any time. The JUMP selections may be made, or dropped, only when the computer is stopped. Select these as follows:

1) SELECTIVE STOPS GROUP - - - SELECT STOP 1 to stop the computer at the end of the current test section (test A, B, C, D, E, F, G, H, I, J, or K).

2) SELECTIVE JUMPS GROUP - - - SELECT JUMP 1 to repeat the current section of the test.

3) SELECTIVE STOPS GROUP - - - SELECT STOP 2 to stop after error address is typed out, or an error bit typeout.

4) SELECTIVE JUMPS GROUP - - - SELECT JUMP 2 to omit further error print out after Stop 2 has been selected, and continue the test. (This avoids time-consuming error typeout where a large number of errors are being found.)

5) SELECTIVE STOPS GROUP - - - SELECT STOP 3 to stop when an error occurs during test J. This is a specific error of a type which might be lost before the normal error check is made.

6) SELECTIVE JUMPS GROUP - - - SELECT JUMP 3 to run SHORT MC Storage Test. (Bypasses error search and tests a2, b2, F, and K.)

Step 3. At the Supervisory Control Panel two switches are used to vary the operating conditions of the MCS System. The AMPLIFIER MARGINAL CHECK group includes a three-position switch labelled MC which places the vacuum tube bias voltage in the MCS system on high, normal, or low when placed at the HI, NORM, or LO positions respectively. (HI bias voltage means high negative voltage.) The REDUCE HEATER group includes a two-position switch labelled MC, which places the MC vacuum tube filament voltage at normal (6.3 volts) or low (5.7 to 5.8 volts). In normal operation this switch is placed in the DOWN position to obtain 6.3 volt filament operation. The usual procedure is to run the MC test in the following order, using the switch settings indicated.

1) Normal margin, normal heater;

2) High margin, normal heater;

3) Lo margin, normal heater;

4) High margin, low heater.

Set the TEST SWITCH GROUP F_1 switch to the up (MD) position and set the "TEST-NORMAL" switch to the up (TEST) position.

Step 4. Operate the MASTER CLEAR button. Operate the START button.

3. THEORY OF THE TEST

Instructions 40000 and 40001 are performed to check the setting of the F_1 switch on the Supervisory Control Panel. This switch must be set to MD, so that F_1 equals the second MD address, 40001. Instruction 40000 inserts 40005 into the v-address of F_1. If F_1 is 40001, instruction 40001 produces a jump to 40005, and the regular MC Storage Test begins. However, if the F_1 switch is set to MC, F_1 is 00000, and instruction 40001 causes a jump to 40002. Instructions 40002 and 40003 introduce a Type Test subroutine that prints "SET SWITCH TO MD". Instruction 40004 produces a stop to allow the maintenance personnel to set the F_1 switch to the MD position. The program then returns to the regular routine.

The MC Storage Test Routine and a detailed explanation of the function of each instruction is contained in Table 3. Instruction codes, addresses, or operands, which are altered by the program, are underlined. The underlined addresses indicated in Table 3 are the addresses which are originally entered in the program. The following paragraphs explain in general the purpose of each MC test section, how each test section works, what results are indicated on the Flexowriter, and how these results are interpreted and used to locate and correct a malfunctioning stage or component in the MCS System.

Each MC test section, except tests C, I, and K, uses a definite repetitive regular pattern which is stored in the entire MCS system. These patterns are chosen to test certain functions of the MCS system, or they are chosen because reading and writing these patterns in the memory is a more severe test of the MCS system than patterns used in normal use of the computer. A description of the various patterns used in the MC Test Routines follows.

The worst pattern (W.P.) obtains its name from the fact that it produces the worst signal/noise ratio condition when it is read or restored in the MCS system. In the worst pattern, each MC address is either all "0's" or all "1's". Table 1 shows the worst pattern. In Table 1 each MC Address designated with a "0" contains all "0's", and each MC address designated by a "1" contains all "1's". The first 400 octal addresses are shown. This 400 octal address pattern is repeated throughout all 10,000 octal addresses. Table 1 shows the actual worst pattern which exists in the cores of each of the 36 core memory planes.

TABLE 1. WORST PATTERN

	00	01	02	03	04	05	06	07	10	11	12	13 thru 66	67	70	71	72	73	74	75	76	77
000XX	0	1	1	0	0	1	1	0	0	1	1	- - - - - - -	0	0	1	1	0	0	1	1	0
001XX	0	1	1	0	0	1	1	0	0	1	1	- - - - - - -	0	0	1	1	0	0	1	1	0
002XX	1	0	0	1	1	0	0	1	1	0	0	- - - - - - -	1	1	0	0	1	1	0	0	1
003XX	1	0	0	1	1	0	0	1	1	0	0	- - - - - - -	1	1	0	0	1	1	0	0	1
004XX thru 076XX																					
077XX	1	0	0	1	1	0	0	1	1	0	0	- - - - - - -	1	1	0	0	1	1	0	0	1

The complement worst pattern (KWP) is the worst pattern with the information at each address complemented. Therefore, Table 1 would show the complement worst pattern if each "0" was replaced by a "1" and each "1" was replaced by a "0". The worst pattern is used in MC Test D, and the complement worst pattern is used in MC Test E so that after the completion of MC Test D and E, each bit of each MC address has been tested by storing both a "0" and a "1" in it.

The circulate worst pattern test is performed by storing the worst pattern in its standard form, as shown in Table 1, and then shifting the pattern one address at a time from the higher order to the lower order addresses until the worst pattern has been restored to its original position. The pattern is restored to its original position after it has been shifted 400 octal addresses.

Crosstalk between digits within the MCS system is a possible cause of error. Crosstalk is the result of inductive and capacitive pickup between wiring associated with the individual digits within the MCS system. The crosstalk may appear when a "1" is read out of a magnetic core address and result in unwanted pickup in other digit-plane circuits. Practically no crosstalk is produced when a "0" is read out, because the signals are of such low amplitude. The maximum amount of crosstalk is developed within a word when all digits of the word contain a "1", except one, which contains a "0". The cumulative effect of the pickup caused by reading out 35 bits containing a "1" may cause the digit containing a "0" to look like a "1" and thus cause an error if this pickup is excessive.

MC Tests G and H are specifically designed to test for crosstalk within the MCS system. These tests use the crosstalk worst pattern (C.T.W.P.). The C.T.W.P. is the same as the W.P. except that one core memory plane has its pattern complemented. This complemented pattern is the K.W.P.

The C.T.W.P. is generated in MC when each MC address contains a word (W) (000 000 000 000 000 000 000 000 000 000 000 001) or a complemented word (K) (111 111 111 111 111 111 111 111 111 111 111 110) stored in the order shown in Table 2. The pattern word (W) is not a test word in Test G and H, but it is used because it happens to be part of the test pattern. The test word (K) is the word used in testing for crosstalk. The C.T.W.P. in Table 2 shows 400 octal addresses containing a word (W), or its complement (K). This 400 octal word pattern is repeated throughout all 10,000 octal addresses.

TABLE 2. CROSSTALK WORST PATTERN

	00	01	02	03	04	05	06	07	10	11	12	13 thru 66	67	70	71	72	73	74	75	76	77
000XX	W	K	K	W	W	K	K	W	W	K	K	- - - - - - -	W	W	K	K	W	W	K	K	W
001XX	W	K	K	W	W	K	K	W	W	K	K	- - - - - - -	W	W	K	K	W	W	K	K	W
002XX	K	W	W	K	K	W	W	K	K	W	W	- - - - - - -	K	K	W	W	K	K	W	W	K
003XX	K	W	W	K	K	W	W	K	K	W	W	- - - - - - -	K	K	W	W	K	K	W	W	K
004XX thru 076XX																					
077XX	K	W	W	K	K	W	W	K	K	W	W	- - - - - - -	K	K	W	W	K	K	W	W	K

A total of 36 different crosstalk patterns is used in both Test G and H to check each bit of the word for pickup from the other 35 bits. MC Test G tests the MCS system for crosstalk using the test word K, in its 36 possible positions, in the half of the MC addresses that contain the test word (K) during this test. MC Test H tests the other half of the MC addresses not tested in MC Test G. The complement crosstalk worst pattern (K.C.T.W.P.) is obtained by using the complement of the pattern shown in Table 2.

The C.T.W.P. and the K.C.T.W.P. are used to obtain both the worst signal to noise ratio condition and the worst crosstalk condition simultaneously in one test. The 36 combinations of the test word K (111 111 111 111 111 111 111 111 111 111 110) are used because they generate the maximum amount of crosstalk between the selected bit of the word tested and all other bits of that word. Each bit of each MC address is tested for its ability to read out a "0", while it is simultaneously under both the worst signal to noise ratio condition and the worst crosstalk condition in Tests G and H.

The regular daily scheduled MC test routines are performed principally for the purpose of locating and replacing defective chassis, stages, tubes, or other electronic components before the computer is placed in normal operation. The MC test routines are run under normal conditions, as well as marginal conditions, each day. The marginal tests are purposely run to cause components which are defective, or are nearly defective, to fail or cause improper operation. Theoretically, the defective or failing components will fail or cause a stage to malfunction when the MC test routines are performed, before they will fail or cause a malfunction when the computer is in normal use, because the MC test routines are purposely designed to be a more severe test of the MCS system, and they are also run on margins which are more severe than normal. These defective components can then be replaced before they fail when the computer is in normal operation.

With the exception of tests C and K, all the MC test routine sections produce an error address and error bit type-out if an error occurs. (The error address type out is actually the X and Y drive line numbers which intersect at the address which failed.) The error address and error bit typeout information can then be analyzed for each MC test section to determine the stages or components which are causing the error, and whether failure is a "1" turning to a "0", or a "0" turning to a "1". A general discussion of how the error address and error bit typeout information should be interpreted follows.

If all failures are in the same digit or digits at several different addresses, the failure is probably connected with the associated digit plane control. The trouble is probably caused by a defective sense amplifier, digit plane control flip-flop, transmission path from MCS → X or X → MCS, or inhibit circuit.

If failures occur in several digits on a single X or Y drive line the trouble is probably connected with the drive line transformer, crystal diodes, or the potentiometer associated with the particular drive line failing.

If failures occur in several digits on every eighth drive line, the trouble is probably connected with the current generator associated with those lines.

If failures occur in several digits, on groups of eight adjacent drive lines, the trouble is probably in the associated current diverters.

Placing the REDUCE HEATER GROUP MC switch in the UP position decreases the filament voltage to 5.7 or 5.8 volts. The UP position is used on marginal checks. When using marginal checks, dropping the filament voltage lowers the emission capabilities of all tubes in the MCS system. However, this has little effect on the non-standard circuits, because their feedback paths compensate for the lowered emission; thus, errors picked up during low filament tests are usually caused by defective tubes in standard circuits. The exception is the feedback tubes in the current generators and inhibit circuits. These feedback tubes cause the X and Y drive line currents and inhibit currents to increase during the Low Heater test if these tubes have low emission. The larger drive line currents and inhibit currents produce larger signals on the sense line, especially larger "0" signals at the sense amplifier.

The HIGH BIAS MARGINAL AMPLIFIER CHECK increases the bias on the cathode follower which feeds the sense amplifier gate tube. This check usually locates stages, tubes, or components which are causing the signal amplitudes to decrease.

The LO BIAS MARGINAL AMPLIFIER CHECK decreases the bias on the tubes. (The bias is made less negative.) Decreasing the bias on the tubes normally induces the high noise levels to cause faulty operation. The high noise levels are sometimes caused by high drive currents which are in turn usually caused by low emission in the feedback tubes, or improper setting of the control rheostat in the switch chassis (58000) or the Digit Plane Control Chassis (58800).

a. START TEST. - When the F_1 switch is set to MD, the START MC TEST portion of the routine produces the typeout "MC TEST", if the regular MC TEST is to be run. If the short MC TEST is to be run, the MJ3 selective jump is selected, and a jump is made which types out "SHORT MC TEST". MD addresses 40031 and 40032 are used to store the indicator word 75 00001 40005 if the worst pattern (W.P.), or the crosstalk worst pattern (C.T.W.P.), has been generated in MD. When these patterns are needed during the MC test routine, these addresses are checked using a 44 instruction, and a jump is made to either write the pattern in MC from MD or generate the pattern in MD before writing the pattern in MC from MD. If the MCS system is working properly when the MC test routines are performed, the worst pattern, and the crosstalk worst pattern, are written much more rapidly

from the MC addresses, and no time is lost writing from MD addresses. The START MC TEST subroutine clears the W.P. drum generation indication address and the C.T.W.P. drum generation indication address at the beginning of the MC test. Subsequent repeated runs of the MC TEST routine are begun at MD addresses 40010. When the MC TEST routine is entered at MD address 40010, the W.P. and C.T.W.P. drum generation indication addresses are not cleared, because the instructions at MD addresses 40006 and 40007 are bypassed. The program then produces a jump to the beginning of TEST A at address 40033.

b. TEST A. - The purpose of Test A is principally to determine whether the MCS system can hold and restore "1's". In order for the MCS system to pass test a1 (hold "1's"), it is necessary for the following logical circuit paths to be functioning properly in the order listed. (Refer to Magnetic Core Storage Block Diagram Dwg. No. XG93068.)

1) Transmission path from X-register → MCS consisting of:

   a) X-register to gates in each digit plane control flip-flop "set" input,

   b) Logical "OR" circuits in each digit plane control flip-flop "set" input,

   c) Digit plane control flip-flop,

   d) Logical "AND" circuit in each Inhibit/Disturb Generator circuit input,

   e) "Set" input of each Write/Restore flip-flop,

   f) Gates V05-071, V03-071, and V07-071.

2) Transmission path from MCS to X-register consisting of:

   a) Sense Amplifier,

   b) Sense Amplifier gates in each digit plane control,

   c) Restore/Read to X Pulse.

Test a1 also tests the complete drive circuits as well as the X and Y drive line currents and the ability of the Inhibit/Disturb generator to turn off. There is no Inhibit current when the Digit Plane Control flip-flop is set to "1".

In test a1, Q is cleared, and a repeated transmit negative command writes "1's" in all MC addresses. Each MC address is transmitted to itself 32 times and then summed in A. The correct sum is then subtracted from A, and A is checked to determine whether it is 0. If A = 0, no error has occurred and the test proceeds to section a2. If A $\neq$ 0, an error has occurred and the program causes "a1" to be typed out. If the SHORT MC TEST is being run, a jump is then taken to repeat test a1 if a1 fails. If the regular MC TEST is being run, the program types out "ones", and prepares the interpret subroutine to test for bits

that failed to hold "1's". A jump is then made to the error search subroutine and the error address X and Y drive line numbers, and the error bit numbers are typed out. After the test a1 error search is completed, test a2 is omitted and the program proceeds to TEST B.

If test a1 passes, the program proceeds to an optional jump to bypass test a2 for SHORT MC TEST. If the regular MC TEST is being run, test a2 produces a repeated command which reads and restores each MC address 32 times, and then checks the sum of each MC address the same as test a1. The remainder of test a2 is the same as test a1. Test a2 does not involve the transmission path from X → MCS. Therefore, if test a1 passes and test a2 fails, the trouble is probably in the logical "OR" circuit in the set input of the Digit Plane Control flip-flops.

c. TEST B. - The transmission paths and logical circuits used during MC TEST B are the same as those used in MC TEST A, except the Inhibit/Disturb current generator circuit. The Inhibit/Disturb current is turned on during MC TEST B, but only the Disturb current is turned on during MC TEST A. MC TEST B is therefore a test of the ability of the Inhibit current to be fully turned on. A failure of Test B, after Test A passes, probably indicates a defective Inhibit/Disturb current generator associated with the Digit Plane Control for those bits which fail. The instructions used in MC TEST B are the same as those used in MC TEST A, except TEST A reads and writes "1's", and TEST B reads and writes "0's".

d. TEST C. - MC TEST C is the MC Address Register test, and it is assumed that all other MCS system logical circuits are working. TEST C cannot pass unless TEST A and TEST B pass, because TEST C uses the same transmission paths X → MCS and MCS → X. However, TEST C is specifically designed to test the ability of the MC Address Register flip-flops to toggle from the "0" to the "1" state, and back again, at high speed. The specific transmission paths tested are AR → SAR and the AR flip-flops.

In TEST C each MC address, 00001 through 07776, is cleared and two pre-stored constants, 25 25252 52777 and 00 01252 52525, are stored in MC addresses 00000 and 07777 respectively. The MC address 00000 is the address contained in the MC Address Register when all its flip-flops are set to "0". The MC address 07777 is the address in the MC Address Register when all its flip-flops are set to "1". A repeated 21 instruction is used, therefore, to toggle these flip-flops 10000 octal times. If the MC address register flip-flops toggle correctly during this instruction, the check sum stored in MC address 00000 is 37 77777 77777. The check sum in MC address 00000 is checked against the correct check sum, using a 43 Equality Jump instruction. If the check sum in MC address 00000 is not correct, the Flexowriter types out c-ar. If the check sum is correct, a jump is made to generate the worst pattern (W.P.) before proceeding to TEST D.

e. GENERATE WORST PATTERN IN MC SUBROUTINE. - The worst pattern is generated in MC first, because it takes much longer to generate it in MD. (It takes .20 seconds to generate the worst pattern in MC and 30 seconds to generate the worst pattern in MD.) The daily MC Test routines are run to obtain a rapid check on the operation of the MCS system. If the MCS system is working properly, the worst pattern is generated in MC. If the MCS system is not working properly,

and the worst pattern cannot be generated in MC, it is generated in MD and then transferred to MC.

The generate worst pattern in MC subroutine first generates the worst pattern in MC. The contents of each MC address are then summed in A, and the sum is shifted left 61 places. The correct check sum is then subtracted from A. If (A) $\neq$ 0, the worst pattern cannot be generated in MC. A jump is made to determine whether the worst pattern has been generated in MD. (The worst pattern could have been generated in MD during a previous run of the test.) If the worst pattern is generated in MD, a jump is made to transfer it to MC. If the worst pattern has not been generated in MD, a jump is made to generate it in MD before transferring it to MC. When the worst pattern has been generated in MC, a jump is made to begin the current test section D, F, or J.

f. TEST D. - The hold worst pattern test uses the same transmission paths as Tests A and B under the worst possible signal to noise ratio condition. Test D is, therefore, a severe test of the ability of the sense amplifier of each Digit Plane Control to distinguish a "1" from a "0" signal. The instructions used in Test D are the same as those used in Test a1.

g. TEST E. - The hold complement worst pattern test is the same as Test D, except it uses the complement worst pattern. The instructions used in Test E are the same as those used in Test a1.

h. TEST F. - The circulate worst pattern test uses the same transmission paths as Tests D and E. Test F checks the ability of the sense amplifier to distinguish a "0" from a "1" under varying noise conditions.

The first instruction is a jump to generate the worst pattern in MC. The circulate worst pattern index is transmitted to Q next, and each MC address is circulated backwards one address. The sum of each MC address is then added to A, and the correct check sum is subtracted from A. If an error occurs the Flexowriter types out "f". The remainder of the circulate worst pattern index is transmitted to the interpret subroutine so that the correct error bits can be determined. The Flexowriter next types out "ciwp", and the program jumps to the error search subroutine. When the error search is completed, a jump is made to end Test F and begin Test G. If no error occurs during Test F, the circulate instructions are repeated 400 octal times, and the worst pattern is back in its original position. A jump is then made to end Test F and begin Test G.

i. TEST G. - Test G uses the crosstalk worst pattern to test the ability of each bit of each MC address to read out a "0" while simultaneously under both the worst signal to noise ratio condition and the worst crosstalk condition. Test G uses the same transmission paths as Tests D and B. The type of crosstalk detected by Tests G and H is usually caused by either poor lead dress or poor grounds.

In Test G an attempt is first made to generate the C.T.W.P. in MC. The C.T.W.P. is then summed in A, and the correct check sum is subtracted from A. If A $\neq$ 0, the C.T.W.P. has not been generated correctly in MC, and a jump is made to generate the C.T.W.P. in MD before it is transferred to MC. If A = 0, the C.T.W.P. has been generated correctly in MC, and the test proceeds to the

next instruction. The hold C.T.W.P. cycle is performed twice, and the contents of MC are then summed in A, and the correct check sum is subtracted from A.

If A ≠ 0, Test G failed and the Flexowriter types out "gctwp". (If the Short MC Test is being run, the Flexowriter types out "g", and Test G is repeated.) The next instruction sets the interpret subroutine to search for W.P. error bits, and then the program converts the C.T.W.P. to the W.P. except for the error bits.

The first test word is next transmitted to Q. The next instruction determines the current position of the complemented bit. The number of the position of the complemented bit is transmitted to the v-portion of instruction 40435, which shifts the original pattern word in Q to the current position. The current C.T.W.P. is converted to the W.P., except for the error bits, and a jump is made to the error search subroutine.

When the restore cycle is completed twice, instructions 40415 through 40417 shift the contents of each MC address to the left one place, and then the hold/restore cycles are repeated. The C.T.W.P. is shifted by the program until each digit has held a "0".

The end Test G instructions produce a stop if MS1 is selected. The next instruction produces a jump to repeat Test G if MJ1 is selected. If neither MS1 or MJ1 is selected, the program proceeds to Test H. If any part of Test G fails, Test G is repeated on the Short MC Test, and the error search subroutine is omitted. If any part of Test G fails on the regular MC Test, the error search subroutine types out the errors, and then the program proceeds to Test H through the use of the end Test G instructions.

j. TEST H. - Test H is the same as Test G except that it uses the K.C.T.W.P. to test the MC addresses which were not tested in Test G. The instructions used in Test H are the same as those used in Test G.

k. TEST I. - The inhibit disturb sensitivity test checks the ability of each core of each MC address to hold the "1" magnetic state after being subjected to 8190 repeated half magnitude demagnetizing pulses. Test I is a severe test of the power supply, because the Inhibit/Disturb current generator is turned on in high speed bursts. Failure of Test I may be caused by excessive ripple or poor regulation of d-c voltages.

The instructions for Test I first transmit "1's" to MC address 00001 through 07777. The next instruction transmits "0's" to MC address 00000. MC address 00000 is then transmitted to itself 4095 times, and then complemented. The contents of each MC address are summed in A, and the correct check sum is subtracted from A. If (A) ≠ 0, the test has failed, and the Flexowriter types out "i". If the SHORT MC TEST is being run, Test I is repeated before the error typeout when any part of Test I fails. If the regular MC TEST is being run, the Flexowriter types "ihds". The next instruction sets the interpret subroutine to search for errors in an all "1's" pattern and jumps to the error search subroutine. After the error search subroutine is completed, a jump is made to end Test I. If A = 0 after the first error check, Test I proceeds to the second part which is the same as the first part except that MC address 03740 is used to read and write "0's". The third part of Test I is the same as the first and

second parts except that MC address 07777 is used to read and write "0's". If an error is produced during Test I, the test always ends after the error search subroutine is completed. The end Test I instructions first produce a stop if MS1 is selected. The next instruction repeats Test I if MJ1 is selected. If MS1 or MJ1 is not selected, a jump is made to Test J.

1. TEST J. - Test J is called the Window Shade Test, because it looks like a window shade on the monitor tube while the test is being run. Test J is similar to Tests D and E except each individual word in MCS is complemented, read and checked, and then restored before the contents of MCS is summed and checked. Test j1 uses the worst pattern (W.P.), and test j2 uses the complement worst pattern (K.W.P.). Test j1 and j2 each consist of two parts. Each individual word in MCS is complemented and restored, and the contents of MCS are summed and checked four times during Test J. The first parts of Tests j1 and j2 use a program which is stored in the first 26 octal addresses of MCS. The second parts of tests j1 and j2 use a program which is stored in the last 28 octal addresses of MCS.

In the first part of test j1 the worst pattern (W.P.) is generated in MCS. The word index 07777-26 (octal) is transmitted to Q. The program of instructions is then transferred to the first 26 octal addresses of MCS, and a jump is made to MCS address 00000. Instruction 00000 complements the word in MC address 00026. Instruction 00001 reads and restores the word in MC address 00026. Instruction 00002 transmits the word to A. Instruction 00003 tests A for 0. If $A \neq 0$, a jump is made to MC address 00004, and the program stops if MS3 has been selected. This stop gives maintenance personnel an opportunity to observe the error in A from the Supervisory Control Panel. Errors of this type may possibly be destroyed when they are recomplemented, and, therefore, could not be found by the error search subroutine. If $A = 0$, the word in MC address 00026 is restored and the program address is advanced to 00027. The word index is then checked and the first 11 instructions are repeated until each MCS address 00026 through 07777 inclusive has been read and restored. The contents of MCS addresses 00026 through 07777 are then summed in A, and the correct check sum is subtracted from A. If $A \neq 0$, the worst pattern is restored in the first 26 octal MC addresses, and the Flexowriter prints "j1", and then proceeds to the error search subroutine to type out the error information. If $A = 0$, the program proceeds to the second part of test j1.

The second part of test j1 performs the same operations as the first part, but the program is stored in the last 24 octal addresses of MCS, and the test word address is decreased by one each time until each MCS address 00000 through 07753 has been used.

The first and second parts of test j2 are the same as the first and second parts of test j1 respectively, but the complement worst pattern (K.W.P.) is stored in MCS.

Test J is repeated when an error occurs during the Short MC Test.

m. TEST K. - Test K is not a magnetic core memory plane test; it is a logical circuitry test of the partial write flip-flops and their gates. Test K is a test of the information flow paths in the magnetic core section only for the W/R 0-14 flip-flop V21-061; the W/R 15-29 flip-flop, V21-071; the Write MCS 0-14 Gate, V07-071; and the Write MCS 15-29 Gate, V03-071.

The W/R 15-29 flip-flop is set, the Write MCS 15-29 Gate is enabled, and the Restore MCS 15-29 Gate is not enabled when the 15 instruction (Transmit U Address) is used. The W/R 0-14 flip-flop and the W/R 30-35 flip-flop are not set during the 15 instruction, and the Write MCS 0-14 and Write MCS 30-35 Gates are not enabled during the 15 instruction. The Restore MCS 0-14 and Restore MCS 30-35 Gates are enabled during the 15 instruction. Test k1 tests the operation of these circuits. The first instruction of test k1 clears Q and A. The next three instructions write "0's" in each MC address. The mixed word (01010101010101010101010101010101010101) is then transmitted to Q, and the test word is transmitted to the u portion of each MC address using a repeated 15 instruction. The contents of each MC address are then summed in A and checked for error. If an error occurs the Flexowriter types "k1 15", and the test proceeds to test k2. If no error occurs in test k1, the program also proceeds to test k2.

Test k2 is the same as test k1, but a repeated 16 instruction is used. The W/R 0-14 flip-flop is set, the Write MCS 0-14 Gate is enabled, and the Restore MCS 0-14 Gate is not enabled when the 16 instruction (Transmit V Address) is used. The W/R 15-29 flip-flop and the W/R 30-35 flip-flop are not set during the 16 instruction, and the Write MCS 15-29 and Write MCS 30-35 Gates are not enabled during the 16 instruction. The restore MCS 15-29 and Restore MCS 30-35 Gates are enabled during the 16 instruction. Test k2 tests the operation of these circuits. If an error occurs during test k2 the Flexowriter types "k2 16" and a jump is made to the End MC Test Subroutine. If no error occurs during test k2, a jump is made immediately to the End MC Test Subroutine.

n. END TEST SUBROUTINE. - The end test subroutine provides a different set of termination instructions for the Regular MC Test and the Short MC Test. The instructions for the regular MC Test produce the typeout "COMPLETED". The next instruction restores the correct instruction at the F1 address, and the program stops. Pushing the start button after the program stops starts the regular MC Test over again.

If the Short MC Test is being run, the End Test Subroutine produces the typeout "END", and the Short MC Test automatically starts over again.

o. ERROR SEARCH SUBROUTINE. - In all test sections which use the error search subroutine except Tests G and H, each MC address contains all "0's" or all "1's", except the error bits.

If an error is detected in any of the MC addresses during Tests G and H, the contents of each MC address are converted to all "0's" or all "1's", except the error bits. A jump is then made to the error search subroutine. Since the error word can be either a positive or a negative number, it is necessary to check each MC address for both positive or negative error words. A repeated 42 Threshold Jump instruction is used to detect errors in each MC address in the error search subroutine. This instruction is used to determine whether the content of each MC address is greater than zero. If the contents of the MC address are greater than zero, a positive error has been found. Negative errors are also detected by this instruction by complementing each MC address when it is transferred to Group 7 of MD. When the contents of each MC address are complemented, a negative error word is changed to a positive error word, and it is also detected by the 42 instruction. The positive and negative error word

addresses are compared as they are detected so that they can be typed out in numerical order.

The error search subroutine first transfers the contents of each MC address to Group 6 of MD. The complement of the contents of each MC address is then transferred to Group 7 of MD. All error search subroutine instructions which are altered by the program are then restored to their original value, and a jump is made to begin the error word search. "A" is cleared first, and a repeated 42 instruction is used to detect a positive error word. If a positive error word is detected, a jump is made to set up the repeated instruction to start at the next address. The positive error word and address are determined and stored. The negative search completion jumpout and the positive processing jumpout are then changed to jump to the error word comparison instructions. The program then clears A, and a jump is made to the negative error word search instructions. If a negative error word is found, it is processed the same as a positive error word, and a jump is made to the error address comparison instructions. The error address comparison instructions use a 42 instruction to determine whether the positive or negative error word address is the larger. The program transfers the smallest error word address and the smallest error word to the interpret subroutine. A return jump is then made to the interpret subroutine which types out the error word address, X and Y drive line numbers, and the error bit numbers. If a positive error word was the smaller, the return jump is made to proceed with the positive error word search. If a negative error word was the smaller, the return jump is made to proceed with the negative error word search. The positive and negative error word search continues in this manner through each MD address in Groups 6 and 7 until the last MD addresses 67777 and 77777 are to be checked.

The last address in MD Group 6 is tested for error using a 42 instruction which is not repeated. If an error is detected in MD address 67777, a jump is made to store the address and the word in temporary storage. The positive error word search beginning instruction is altered to produce a jump back to the current test section, and a jump is made to the next step. The next step is determined by the progress of the search.

If no error is found in the last address of MD Group 6, the octal number 10000 is transferred to the positive error address temporary storage location. If any negative error words are found subsequent to the completion of the positive error word search, the error word address will always cause only the negative error word addresses to be typed out in the proper order because they are being compared with the octal number 10000 which is larger than any MC address. The next instruction alters the negative error search termination jump to jump back to the current test section, and a jump is made to continue the test. Group 7 is processed in the same manner as the last address in MD Group 6.

p. MD GENERATION SUBROUTINE. - The MD generation subroutines are used by the MC Test Routine when the test patterns cannot be generated directly in MC. If the worst pattern (W.P.) cannot be correctly generated directly in MC, the contents of MD address 40031 are transmitted to Q. A 44 Q Jump instruction is used next to test the contents of Q_{35}. If the worst pattern has been generated in MD, the contents of MD address 40000 are stored in MD address 40031, and Q_{35} is a "1". Therefore, the Q Jump instruction produces a jump to the transfer W.P. to MC sequence of the MD generations subroutine. If the worst

pattern has not been generated in MD, Q_{35} is a "0", and a jump is made to MD address 40222 which is a return jump instruction. The return jump instruction jumps out to generate the worst pattern in MD before transferring it to MD.

The crosstalk worst pattern (C.T.W.P.) is controlled in a similar manner except that the C.T.W.P. generation indication is stored in MD address 40032. The W.P. and C.T.W.P. are not generated in MD each time they are needed, because it takes approximately 35 seconds to generate each pattern. If the pattern is already generated in MD, this time is saved.

The MD generation subroutines consist of six separate sequences: generate W.P. in MD, generate C.T.W.P. in MD, transfer W.P. to MC, transfer K.W.P. to MC, transfer C.T.W.P. to MC, and transfer K.C.T.W.P. to MC. Each sequence has a separate entrance and exit instruction. Since both the W.P. and C.T.W.P. are identical in each quarter section, only one fourth of each pattern is generated in MD. This leaves the remainder of MD Group 5 available for other programs.

The generate W.P. in MD sequence first clears Q and A. All "1's" are then transmitted to MD address 56000, and all "0's" are transmitted to MD address 56001. A repeated transmit negative instruction is used next to generate the worst pattern in MD addresses 54002 through 54177. A second repeated transmit negative instruction is then used to generate the worst pattern in MD addresses 54200 through 55777 inclusive. The next instruction transmits the W.P. generation in MD indication to MD address 80031, and a jump is made back to the test.

The generate C.T.W.P. in MD sequence is the same as the generate W.P. in MD sequence, except that the pattern word (W) is used. The C.T.W.P. generation in MD indication is transmitted to MD address 40032 and a jump is made back to the test.

Each transfer sequence uses a series of four separate repeated instructions, because the required pattern is generated in MD in only one fourth of the required addresses. The transfer W.P. to MC sequence and transfer C.T.W.P. to MC sequences use a repeated transmit positive instruction. The transfer K.W.P. to MC sequence, and transfer K.C.T.W.P. to MC sequences use a repeated transmit negative instruction.

q. INTERPRET SUBROUTINE. - The interpret subroutine types out the X and Y drive line numbers and error bit numbers of the error words after they are detected by the error search subroutine. The interpret subroutine determines whether the error word should be all "0's" or all "1's", and then detects the error bits if one of the worst patterns has been used. The X and Y drive line numbers are always typed out first. After the X and Y drive line numbers are typed, the program produces a jump to one of five different sequences depending on the test pattern used, i.e., hold "1's", hold "0's", hold W.P., hold K.W.P., or circulate W.P. (The C.T.W.P. and K.C.T.W.P. test patterns are converted to W.P. or K.W.P. respectively, except for the error bits, by the individual test section before the error search subroutine is used.) Three separate sequences are used to determine the correct error bit content for the worst patterns, W.P., K.W.P., and circulate W.P., before typing out the error bit numbers. The error bit interpret sequence used by the program is determined by the individual test section, which prestores the proper jump address in the jump instruction at MD address 41343 before jumping out to begin the error search subroutine.

The hold "1's" test section (Test A) sets the interpret subroutine to search for "0" error bits, and then jumps to the error search subroutine. The error search subroutine detects the error words and their addresses, and produces a jump to the interpret subroutine. The interpret subroutine transmits the error address to a temporary storage location, and then transmits the error address to Q and shifts Q left 30 places. This places the Y drive line numbers of the error address in bits 0 through 5 of Q. The next instruction transmits the Y drive line numbers to A. The Flexowriter then types out "y", and a jump is made to a sequence which converts the binary Y drive line number to a decimal number.

The first instruction of the binary to decimal conversion sequence divides (A) by 10 (12 octal) to convert to the decimal equivalent. The remainder is stored in A after the divide instruction, and a 35 instruction is used next to add the remainder to the prestored operand at MD address 41416 and transmit the sum to MD address 41422. (This operand is a basic type instruction which will type out the number code stored at MD address 41456. A series of decimal type out codes are prestored at MD addresses 41456 through 41467 in ascending order from 0 through 9. Therefore, adding any number from 0 through 9 to the basic typeout instruction sets this instruction to type out the numbers 0 through 9 respectively.) The most significant decimal digit of the Y drive line is stored in Q; therefore, Q is transmitted to A and another 35 instruction is used to set the typeout instruction for this digit and store it at MD address 41417. The Flexowriter then types the most significant Y digit. The program then transmits the current error word to Q and the bit index to A. (The bit index in A is only necessary when the decimal typeout sequence is used for error bits.) The Flexowriter then types the least significant Y drive line digit. An optional MJ2 stop instruction is used at this point to allow maintenance personnel to set an MJ2 jump, if it is desired to eliminate further error typeout. An MJ2 jump instruction is used after the stop instruction, which jumps the program back to the end of the current test section when it is selected.

The program then proceeds to interpret the X drive line in the same manner as the Y drive line if MJ2 has not been selected. After the X drive line digits are typed out, a jump is made to interpret the error bits of the error word.

The interpret error bit sequence for the hold "1's" pattern first transmits the complement of the error word to Q. Therefore, all error bits are "1's", and all correct bits are "0's". The bit index is then transmitted to Q. A 44 Q Jump Instruction is used to detect the error bits. If a "1" is in the leftmost bit of Q, Q is negative, an error bit has been detected, and a jump is made to the decimal typeout sequence to type out the decimal number of the error bit. If a "0" is in the leftmost bit of Q, Q is positive, a correct bit has been tested, and a jump is made to the next step. (The 44 instruction always shifts the error word to the left one place.) The next step subtracts 1 from the bit index and jumps to another Q jump instruction to test the next bit, if the index is still positive. If the bit index goes negative, all bits have been tested and the interpret subroutine is terminated. The same instruction sequence is used to detect the error bits for each test pattern.

The hold "0's" test section sets the interpret subroutine to search for "1" error bits before jumping to the error search subroutine. The only difference between the hold "1's" interpret subroutine sequence and the hold "0's" interpret subroutine sequence is that the error word is transmitted positive to Q.

The same instructions are used to convert the X and Y drive line numbers and detect the error bit numbers for the test patterns W.P., K.W.P., and circulate W.P. However, the interpret subroutine determines whether the error word should be all "0's" or all "1's" before using the error bit number sequence when these test patterns are being used.

The worst pattern is shown in Table 1. The pattern is stored in the MC addresses in the repeated pattern 0110, 0110, 0110, etc., for each group of four MC addresses on Y drive lines Y_0, Y_1; Y_4, Y_5; Y_8, Y_9; etc. to Y_{60}, Y_{61}. The pattern is stored in the repeated pattern 1001, 1001, 1001, etc., for each consecutive group of four MC addresses on Y drive lines Y_2, Y_3; Y_6, Y_7; Y_{10}, Y_{11}; etc., to Y_{62}, Y_{63}. The symmetry of the pattern is used in the interpret subroutine to determine whether the error word should be all "0's" or all "1's". Four error bit code words are used which look the same as the worst pattern for the first seven addresses of the Y drive lines Y_0, Y_1, Y_2, and Y_3. These code words are stored in MD addresses 41440 through 41443. Only the first four addresses of the first four Y drive lines are actually required. In the binary number system the two least significant bits are repeated for every group of four consecutive numbers. Therefore, the error bit code word is shifted to the left in Q, according to the two least significant digits of the X drive line number, to determine whether the error word should be all "0's" or all "1's". The error bit code word used is determined by the two least significant digits of the Y drive line number.

The hold W.P. test prestores the MD address 41354 in the jump instruction at MD address 41343. The program then proceeds to determine whether the error bits should be all "0's" or all "1's". The instruction at MD address 41354 stores the error word address. The next instruction left shifts the error word address in Q nine places. The basic error bit code word transfer instruction is transmitted to A, and the two least significant binary bits of the Y drive line number are added to the u portion of Q, and (Q) is stored at MD address 41363. The next instruction transmits the basic shift instruction to A. The error word address is then shifted back to its original position. The two least significant binary bits of the X drive line number are then added to the basic shift instruction, and it is stored at MD address 41364. The above determined error bit code word transfer instruction is used next to transfer the correct code word to Q. The above determined shift instruction left shifts the code word the number of places determined by the two least significant bits of the X drive line number. The next instruction is a 44 Q Jump Instruction, which causes the error word to be transmitted positive to Q, if the error word should be all "0's", or causes the error word to be complemented when it is transmitted to Q, if the error word should be all "1's". The program then proceeds to test the error word bits for errors using the same instruction sequence that was used to test the hold "0's" and hold "1's" error words.

The hold K.W.P. test section prestores the MD address 41431 in the jump instruction at MD address 41343. The interpret subroutine then proceeds to MD address 41431 after the X and Y drive line numbers have been typed out. The instruction at MD address 41431 transmits the error word address to MD address 41452. The next instruction left shifts the error word address in Q nine places. The basic <u>complement</u> error bit code word transfer instruction is then transmitted to A, and a jump is made to MD address 41357. The rest of the sequence is the same as the W.P. sequence. However, the error bit code word transfer instruction used with the K.W.P. sequence is a transmit negative instruction.

The circulate W.P. test prestores the MD address 41344 at MD address 41343. The interpret subroutine then proceeds to MD address 41344 after the X and Y drive line numbers have been typed out. The instruction at MD address 41344 transmits the error word address to MD address 41452. The next instruction transmits the original circulate worst pattern index to MD address 41447. The remainder of the circulate worst pattern index was previously stored at MD address 41437 by the circulate worst pattern test. The next instruction subtracts the remainder of the circulate worst pattern index from the original index to obtain the number of times the worst pattern has been circulated. The next instruction adds the worst pattern circulation count to the error word address to obtain the original address of the error word. A jump is then made to MD address 41355, and the rest of the interpret subroutine for the circulate worst pattern is the same as the interpret worst pattern subroutine sequence.

r. TYPE TEXT SUBROUTINE. - The type text subroutine is used by the MC Test Routine to type out words of more than two letters. A return jump instruction is always used to enter and leave the type text subroutine.

The address of the first type text code letter group is transmitted to the u portion of Q, and the index of the type text code letter groups is transmitted to the v portion of Q prior to jumping into the type text subroutine. The first instruction of the type text subroutine transmits the MD address of the first type text code letter group to the u portion of MD address 41504. The next instruction transmits the index of the type text code letter group to the v portion of MD address 41513. The code letter index is then transmitted to Q. (This index is a series of binary numbers 000001. Each time a letter is typed this index is checked and shifted to the left one place by using a 44 Q Jump instruction. The index in Q_{35} is 1 after the sixth character is typed out, and the type text subroutine is either terminated or a new type code letter group is transmitted to A to be typed out.) The next instruction transmits the first type code letter group to A. The Flexowriter types out the first type code. The contents of A_R are then cleared and shifted to the left six places. The type text subroutine continues to type out the type code group characters until Q_{35} is 1. When Q_{35} is 1, a jump is made to add 00001 to the address of the first code letter group at MD address 41504. The next instruction subtracts 1 from the index and checks the code letter group index. If the index is still positive, a new type text code letter group is transmitted to A, and the sequence is repeated. If the index is negative, the type text subroutine is terminated, and the return jump is made back to the test.

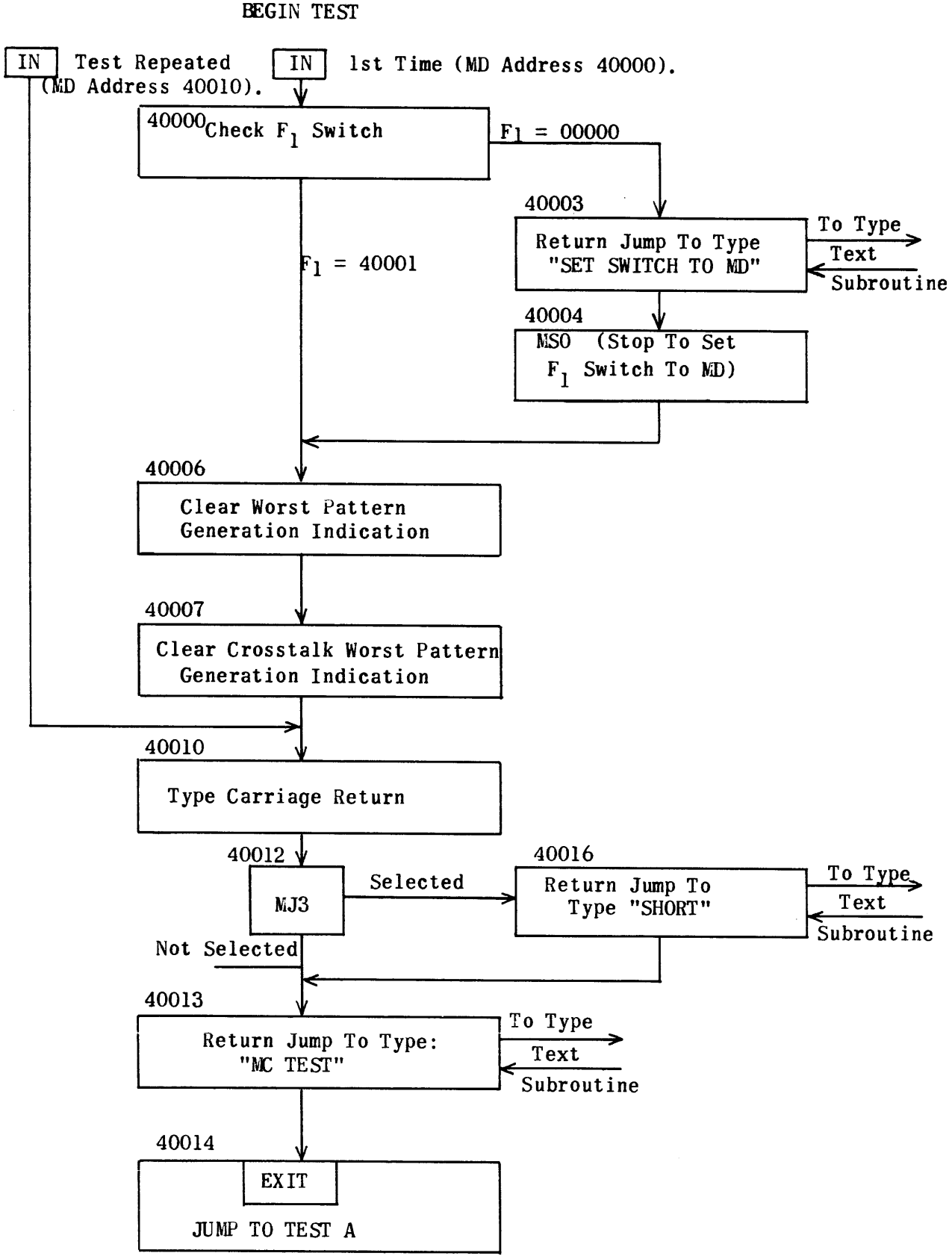


Figure 1. Begin MC Test Routine Flow Chart
PX 142

TABLE 3. MC TEST ROUTINE

PROGRAM: MC Storage Test

DESCRIPTION: Description of each test section within program.

ADDRESS	OP-CODE	u	v	FUNCTION
				Sense F_1 Switch Position.
40000	75	00001	40005	Insert address 40005 in the v-portion of F_1. If F_1 is set to MD, the v-portion of address 40001 is changed to 40005, and a jump is made to address 40005. If F_1 is set to MC, a jump is made to address 40002.
40001	45	00000	40002	If F_1 = 40001, jump to 40005; if F_1 = 00000 jump to 40002.
40002	11	40025	31045	Transmit type text subroutine parameter to Q.
40003	37	41512	41501	Jump to type text subroutine and type out "SET SWITCH TO MD".
40004	56	00000	40005	Stop to set F_1 switch to MD.
				Identify Test
40005	23	31000	31000	Clear Q and A.
40006	11	31000	40031	Clear drum generation indication for worst pattern.
40007	11	31000	40032	Clear drum generation indication for cross-talk worst pattern.
40010	61	00000	40002	Type carriage return.
40011	45	30000	40015	Jump to type "SHORT", if MJ3 is selected.
40012	11	40020	31000	Transmit type text subroutine parameter to Q.
40013	37	41512	41501	Jump to type out "MC TEST".

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40014	45	00000	40033	Jump to Test A.
40015	11	40023	31000	Transmit type text subroutine parameter to Q.
40016	37	41512	41501	Jump to type out "SHORT".
40017	45	00000	40012	Jump to type "MC TEST".
40020	00	40021	00001	Type text subroutine parameter for "MC TEST".
40021	04	47070	41604	Flex type out code for "MC TEST".
40022	01	20240	15704	
40023	00	40024	00000	Type text subroutine parameter for "SHORT".
40024	47	24050	31201	Flex type out code for "SHORT".
40025	00	40026	00002	Type text subroutine parameter for "SET SWITCH TO MD".
40026	45	47242	00104	Flex type out code for: "SET SWITCH TO MD".
40027	24	31140	11605	
40030	04	01030	40722	
40031	00	00000	00000	Worst pattern drum generation indication.
40032	00	00000	00000	Crosstalk worst pattern drum generation indication.

MAGNETIC CORE STORAGE TEST
Test A. Hold Restore "1's" Test

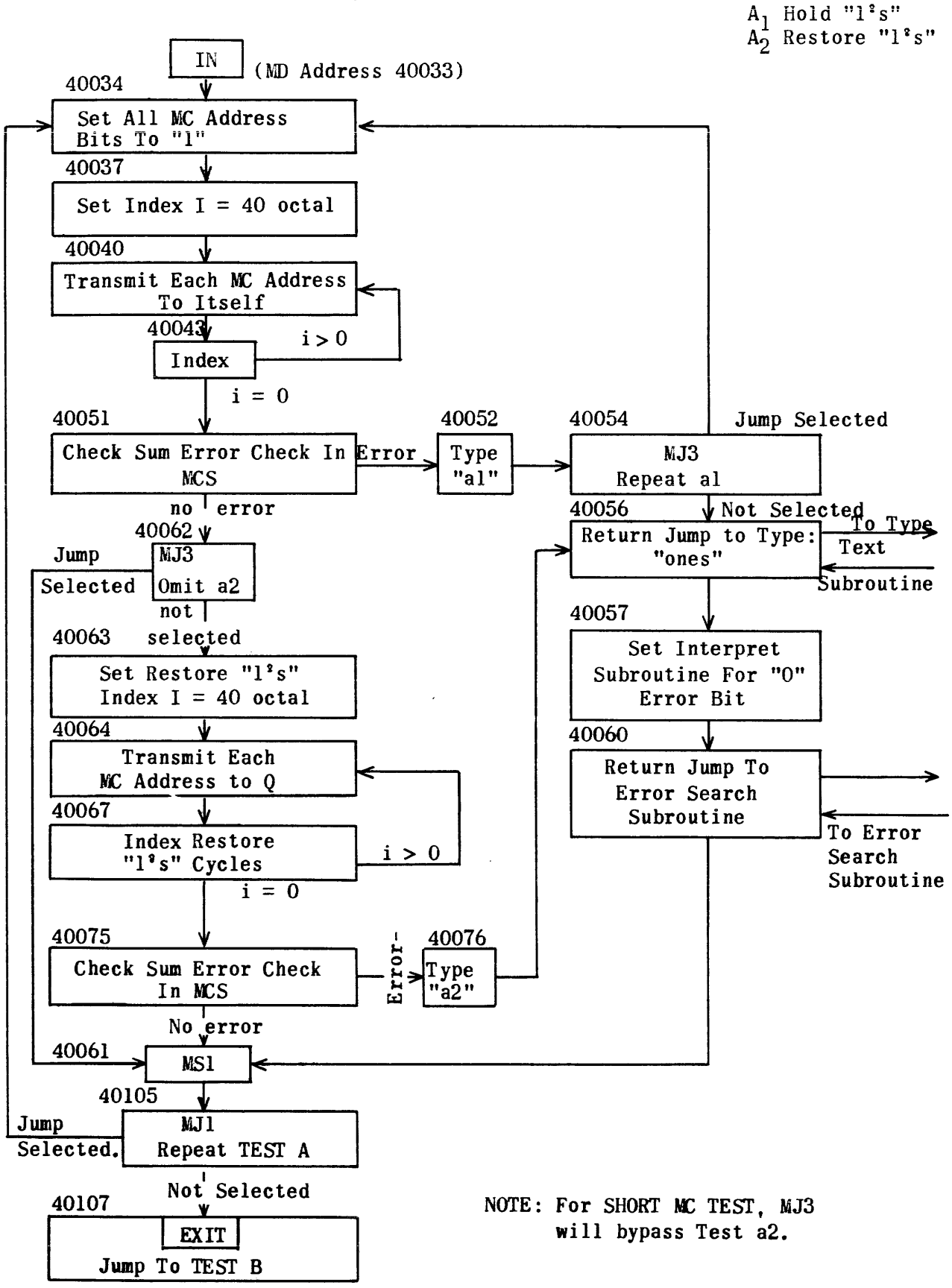


Figure 2. Test A Hold Restor "1's" Flow Chart of MC Test Routine
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS		u	v	FUNCTION
				TEST A
40033	23	31000	31030	Clear Q and A.
40034	75	17777	40036	
40035	13	31000	00000	Transmit "1's" to each bit of each MC Address.
40036	13	31000	07777	
40037	11	40103	31052	Set index No. in Q
40040	75	37777	40042	
40041	11	00000	00000	Read and write contents of each MC Address to itself.
40042	11	07777	07777	
40043	41	31000	40040	Perform cycle 32 times.
40044	23	31000	31074	Clear Q and A.
40045	75	27777	40047	
40046	32	00000	00000	Sum MC contents in A and shift A left 60 places.
40047	32	07777	00074	
40050	34	40104	00000	Subtract correct check sum.
40051	47	40052	40062	Check for error. If A $\neq$ 0, test a1 failed. Type "a1 ones" (on Short MC Test Type "a1" and repeat test a1). If A = 0, proceed to test a2.
40052	61	00000	40033	Type "a1".
40053	61	00000	40037	
40054	45	30000	40033	Repeat test a1 if a1 fails on Short MC Test.
40055	11	40101	31000	Transmit type text subroutine parameters to Q
40056	37	41512	41501	Jump to type text subroutine to type "ones".
40057	16	41475	41343	Prepare interpret subroutine to search for "0" error bit.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40060	37	41151	41104	Jump to error search subroutine.
40061	45	00000	40105	Jump to terminate Test A.
40062	45	30000	40105	Bypass test a2 on Short MC Test.
40063	11	40103	32000	Index to A.
40064	75	27777	40066	Read and restore contents of each MC address.
40065	11	00000	31000	
40066	11	07777	31000	
40067	41	32000	40064	Perform cycle 32 times.
40070	23	31000	31000	Clear Q and A.
40071	75	27777	40073	Sum MC contents in A and shift A left 60 places.
40072	32	00000	00000	
40073	32	07777	00074	
40074	34	40104	00000	Subtract correct check sum.
40075	47	40076	40105	Check for error. If A≠0, type "a2 ones" and jump to error search subroutine. If A=0, jump to end Test A and begin Test B.
40076	61	00000	40033	Type "a2".
40077	61	00000	40044	
40100	45	00000	40055	Jump to type "ones".
40101	00	40102	00000	Type text subroutine parameter for "ones".
40102	04	03062	02445	Flex type out code for "ones".
40103	00	00000	00037	Index for repeated instruction cycle for tests A, B, D, E, G, and H.
40104	77	77777	77777	Correct check sum for tests, A,D,E,F,G,H, and I.
40105	56	10000	40106	Stop after Test A if MS1 is selected.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40106	45	10000	40033	Optional jump to repeat Test A if MJ1 is selected.
40107	45	00000	40110	Jump to Test B.

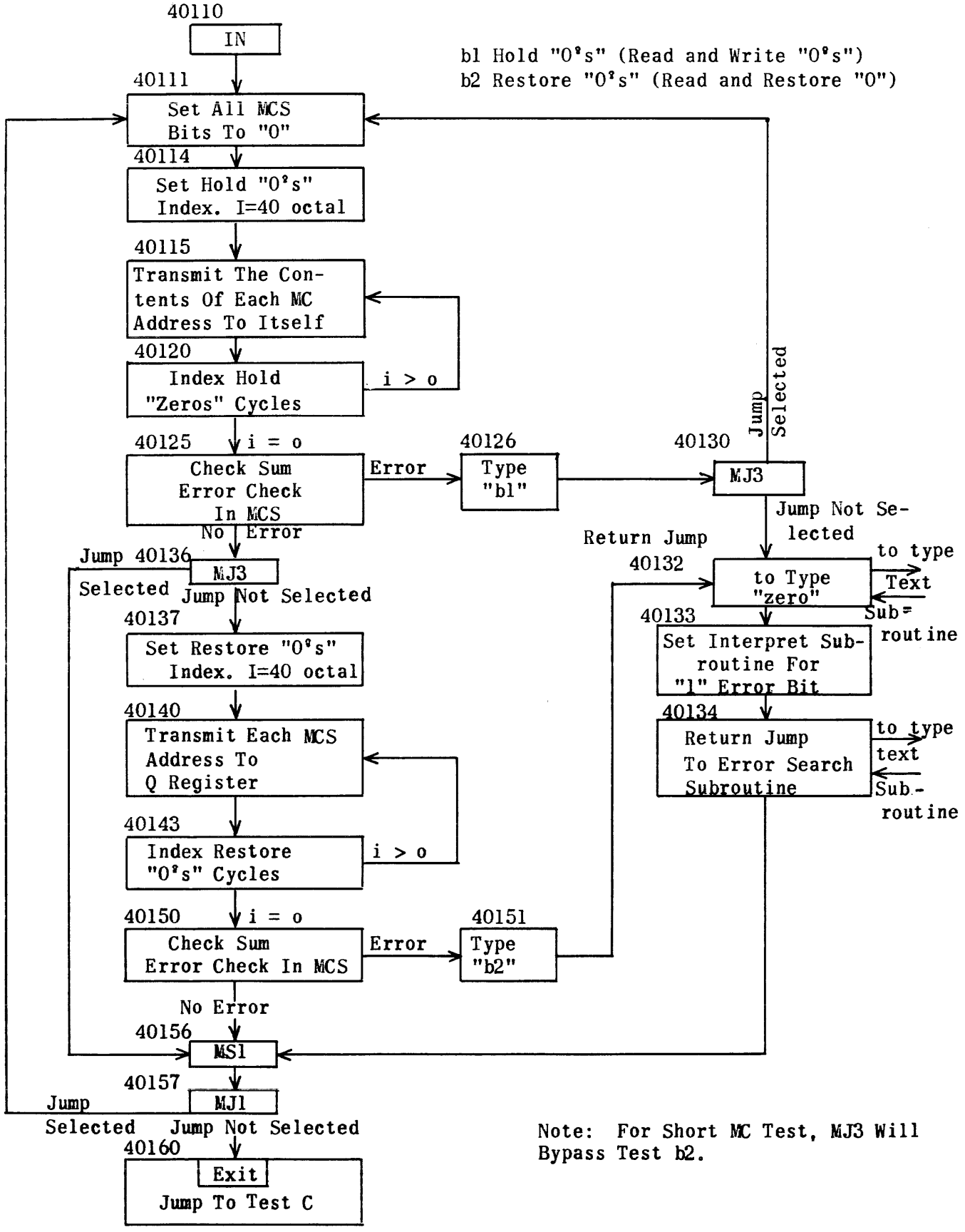


Figure 3. Test B Flow Chart of MC Test Routine
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST B
40110	23	31000	31023	Clear Q and A.
40111	75	17777	40113	Transmit "0's" to each MC address.
40112	11	31000	00000	
40113	11	31000	07777	
40114	11	40103	31052	Index to Q.
40115	75	37777	40117	Read and write contents of each MC address to itself.
40116	11	00000	00000	
40117	11	07777	07777	
40120	41	31000	40115	Perform cycle 32 times.
40121	23	31000	31074	Clear Q and A.
40122	75	27777	40124	Sum MC contents in A.
40123	32	00000	00000	
40124	32	07777	00000	
40125	47	40126	40136	Check for error. If A≠0, type "b1 zero" (on Short MC Test type b1 and repeat test b1). If A = 0, jump to test b2.
40126	61	00000	40110	Type "b1".
40127	61	00000	40114	
40130	45	30000	40110	If test b1 fails, repeat test b1 on Short MC Test.
40131	11	40154	31000	Transmit type text subroutine parameter to Q.
40132	37	41512	41501	Jump to type text subroutine to type "zero".
40133	16	41470	41343	Prepare interpret subroutine to search for "1" error bit.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40134	37	41151	41104	Jump to error search subroutine.
40135	45	00000	40156	Jump to end Test B.
40136	45	30000	40156	Jump to omit test b2 on Short MC Test.
40137	11	40103	32000	Index to A.
40140	75	27777	40142	Read and restore contents of each MC address.
40141	11	00000	31000	
40142	11	07777	31000	
40143	41	32000	40140	Perform cycle 32 times.
40144	23	31000	31000	Clear Q and A.
40145	75	27777	40147	Sum MC contents in A.
40146	32	00000	00000	
40147	32	07777	00000	
40150	47	40151	40156	Check for error. If A≠0, type "b2 zero" and jump to error search subroutine. If A = 0, jump to end Test B.
40151	61	00000	40110	Type "b2"
40152	61	00000	40121	
40153	45	00000	40131	Jump to type "zero".
40154	00	40155	00000	Type text subroutine parameter for "zero".
40155	04	21201	20345	Flex type out code for "zero".
40156	56	10000	40157	Optional stop after Test B.
40157	45	10000	40110	Optional jump to repeat Test B.
40160	45	00000	40161	Jump to Test C.

MAGNETIC CORE STORAGE TEST
TEST C. ADDRESS REGISTER TEST

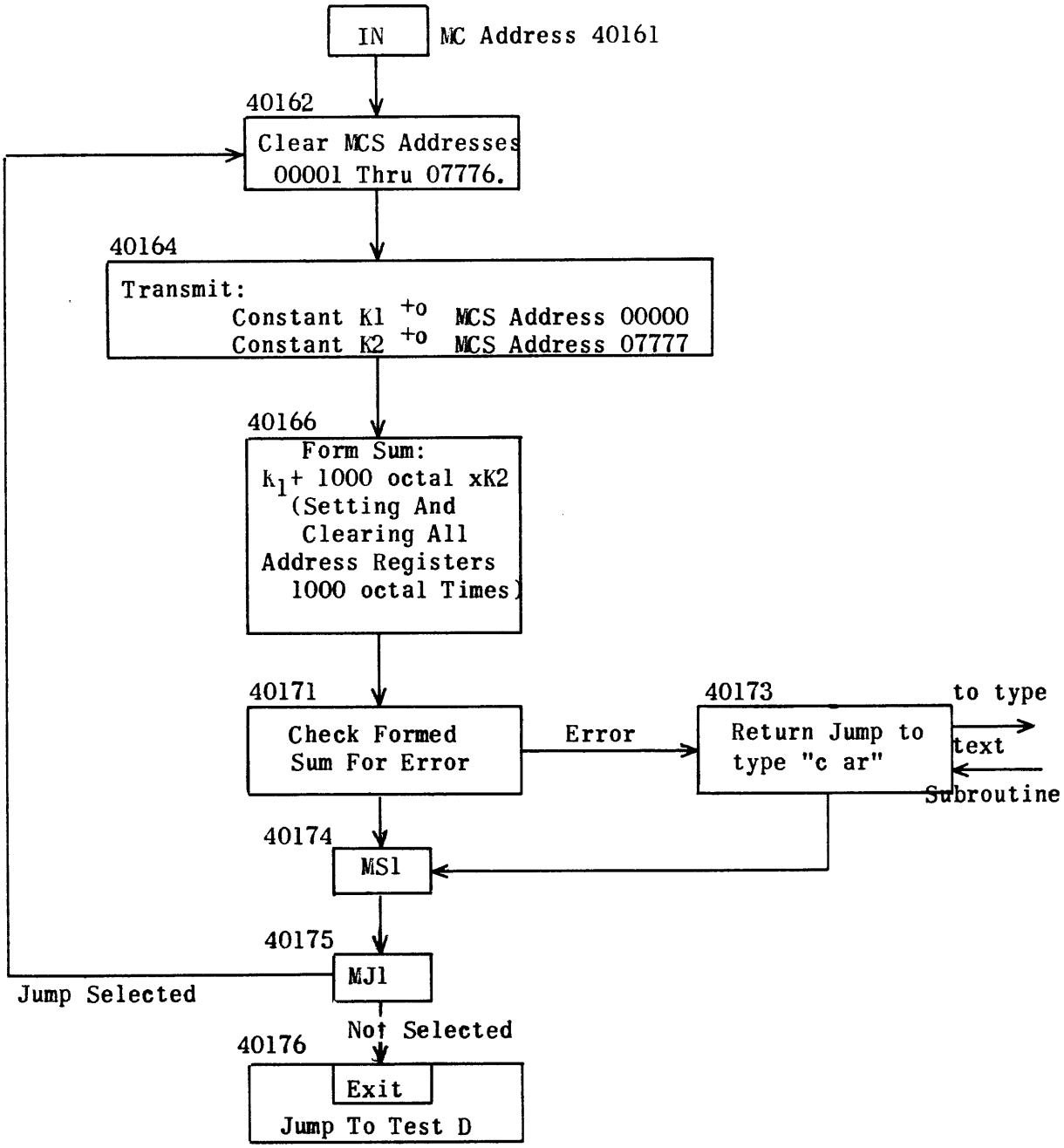


Figure 4. Test C Flow Chart of MC Test Routine
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST C
40161	23	31000	31016	Clear Q and A.
40162	75	17776	40164	Clear MC addresses 00001 thru 07776.
40163	11	31000	00001	
40164	11	40201	00000	Transmit constants to MC addresses 0000 and 07777.
40165	11	40202	07777	
40166	75	01000	40170	Form the check sum and toggle the address register flip-flops.
40167	21	00000	07777	
40170	31	00000	00000	Transmit check sum to A.
40171	43	40203	40174	If an error, type "C-AR". If no error, jump to test D.
40172	11	40177	31000	Transmit type text subroutine parameter to Q
40173	37	41512	41501	Jump to type text subroutine to type "c ar".
40174	56	10000	40075	Optional stop after Test C.
40175	45	10000	40161	Optional jump to repeat Test C.
40176	45	00000	40225	Jump to Test D.
40177	00	40200	00000	Type text subroutine parameter for "c ar".
40200	16	04301	20445	Flex type out code for "c ar".
40201	25	25252	52777	Constants.
40202	00	01252	52525	
40203	37	77777	77777	Check sum.

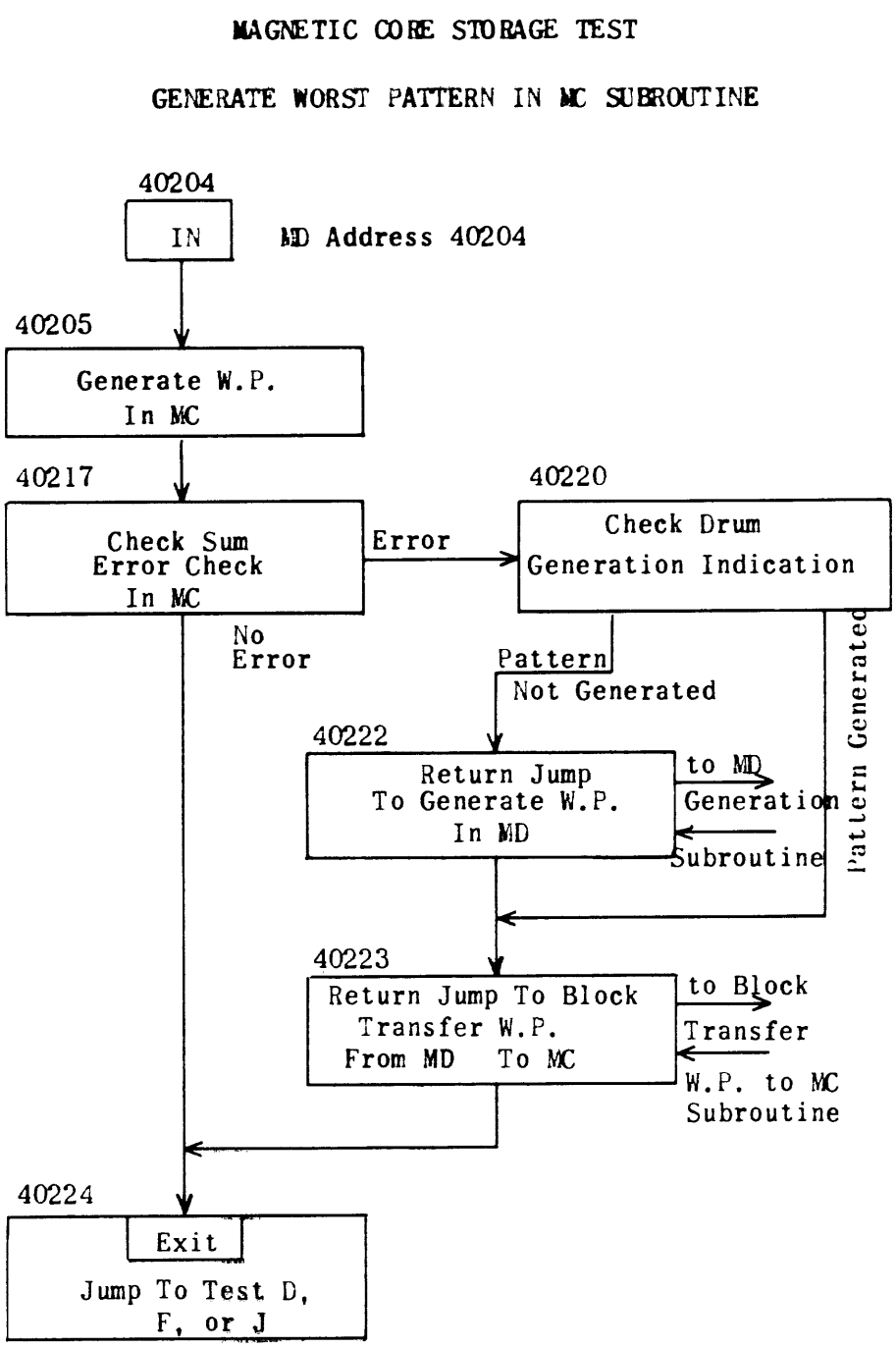


Figure 5. Generate Worst Pattern in MC Subroutine Flow Chart of MC Test Routine
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				Generate Worst Pattern in MC Subroutine
40204	23	31000	31022	Clear Q and A.
40205	11	31000	00000	Generate worst pattern (W.P.) in MCS.
40206	13	31000	00001	
40207	75	30176	40211	
40210	13	00000	00002	
40211	75	37600	40213	
40212	13	00000	00200	
40213	75	27777	40215	Sum MC contents in A, and shift A left 61 places.
40214	32	00000	00000	
40215	32	07777	00075	
40216	34	40104	00000	Subtract the correct sum from A.
40217	47	40220	40224	Check for error. If A $\neq$ 0, W.P. has not been generated correctly in MC; jump to generate W.P. in MD. If A = 0, W.P. is generated correctly in MC. Jump to TEST D, F or J.
40220	11	40031	31000	Check if W.P. is generated in MD. If W.P. is in MD, jump to transfer W.P. in MC; if not, jump to generate W.P. in MD.
40221	44	40223	40222	
40222	37	41254	41244	
40223	45	00000	41265	
40224	45	00000	40226	Jump to TEST D, F, or J (v address altered by program).

MAGNETIC CORE STORAGE TEST

TEST D. HOLD WORST PATTERN (W.P.)

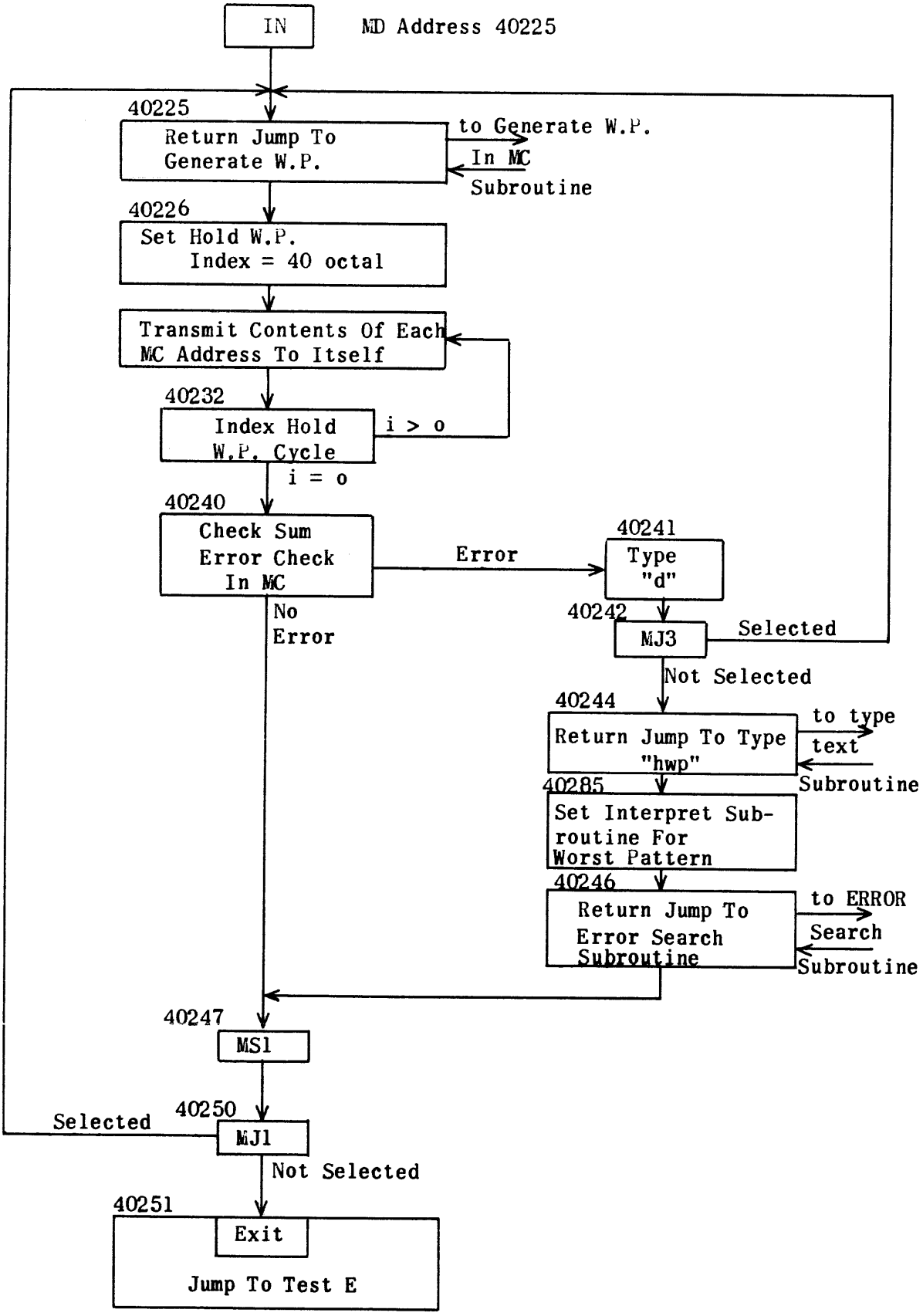


Figure 6. Test D Flow Chart of MC Test Routine
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST D
40225	37	40224	40204	Jump to generate W.P. in MC.
40226	11	40103	31000	Set index in Q.
40227	75	37777	40231	Read and write contents of each MC address to itself.
40230	11	00000	00000	
40231	11	07777	07777	
40232	41	31000	40227	Perform Cycle 32 times.
40233	23	31000	31000	Clear Q and A.
40234	75	27777	40236	Sum MC contents in A, and shift A left 61 places.
40235	32	00000	00000	
40236	32	07777	00075	
40237	34	40104	00000	Subtract correct check sum from A.
40240	47	40241	40247	Check for error. If A≠0, test d failed. Type "d hwp" (on Short MC Test Type "d" and repeat Test D). If A = 0, continue the test.
40241	61	00000	40204	Type "d".
40242	45	30000	40225	If Test D fails, repeat Test D on Short MC Test.
40243	11	40252	31000	Transmit type text subroutine parameter to Q.
40244	37	41512	41501	Jump to type text subroutine to type "hwp".
40245	16	41476	41343	Set interpret subroutine to search for W.P. error bits.
40246	37	41151	41104	Jump to error search subroutine.
40247	56	10000	40250	Stop after Test D if MS1 is selected.
40250	45	10000	40225	Repeat Test D if MJ1 is selected.
40251	45	00000	40275	Jump to Test E.
40252	00	40253	00000	Type text subroutine parameter for "hwp".
40253	04	05311	50445	Flex type out code for "hwp".

MAGNETIC CORE STORAGE TEST

GENERATE COMPLEMENT WORST PATTERN IN MC SUBROUTINE

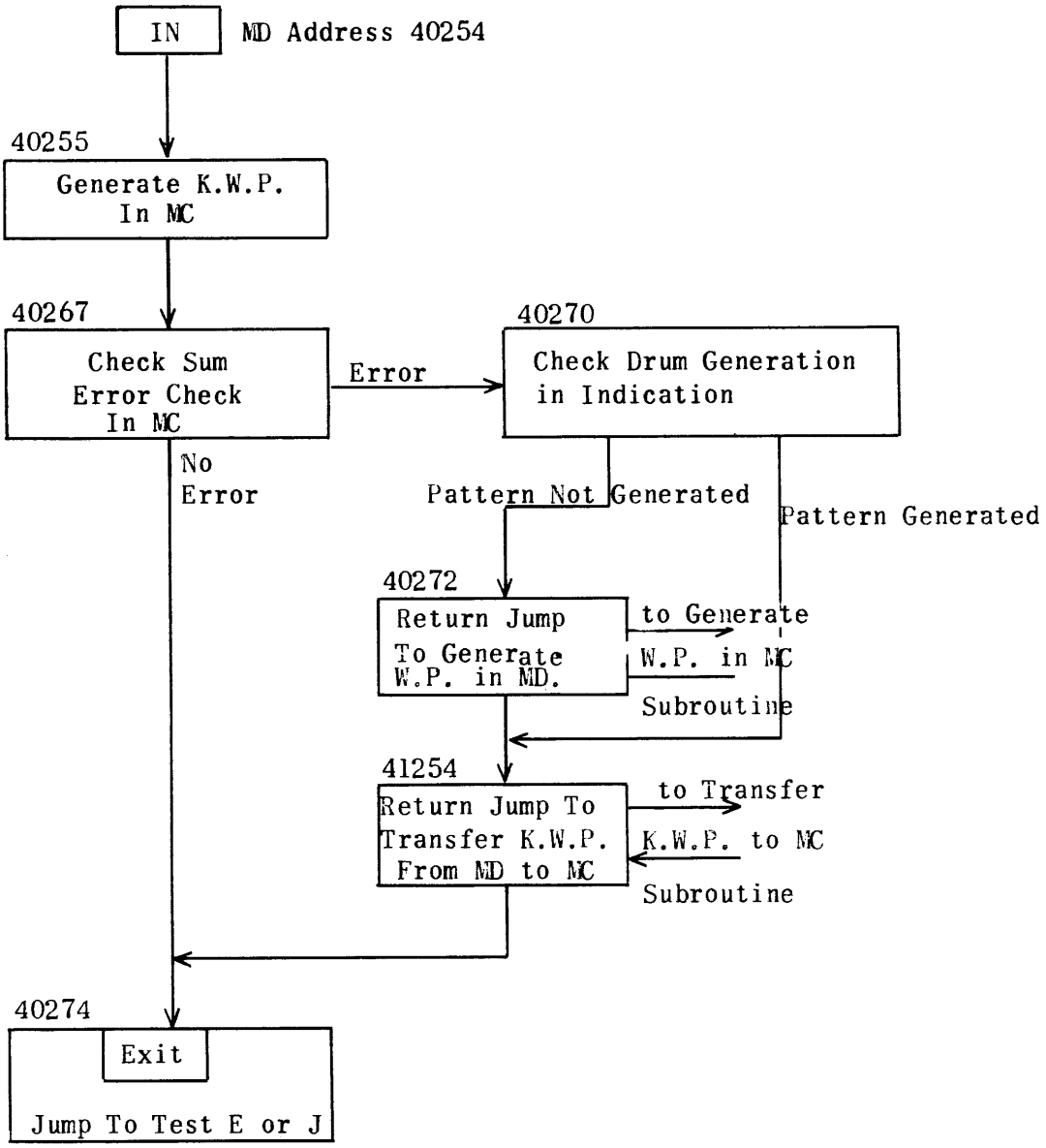


Figure 7. Generate Complement Worst Pattern In MC Subroutine Flow Chart of MC Test Routine PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				Generate Complement Worst Pattern In MC Subroutine
40254	23	31000	31020	Clear Q and A.
40255	13	31000	00000	Generate complement worst pattern (K.W.P.) in MCS.
40256	11	31000	00001	
40257	75	30176	40261	
40260	13	00000	00002	
40261	75	37600	40263	
40262	13	00000	00200	
40263	75	27777	40265	Sum MC contents in A, and shift A left 61 places.
40264	32	00000	00000	
40265	32	07777	00075	
40266	34	40104	00000	Subtract the correct sum from A.
40267	47	40270	40274	Check for error. If A $\neq$ 0, K.W.P. has not been generated correctly in MC; jump to generate W.P. in MD. If A = 0, K.W.P. is generated in MC; jump to Test E or J.
40270	11	40031	31000	Check if W.P. is generated in MD. If W.P. is in MD, jump to transfer K.W.P. to MC; if not, jump to generate W.P. in MD.
40271	44	40273	40272	
40272	37	41254	41244	
40273	45	00000	41276	
40274	45	00000	40717	Jump to Test E or J (v address altered by program).

MAGNETIC CORE STORAGE TEST
TEST E. HOLD COMPLEMENT WORST PATTERN (K.W.P.)

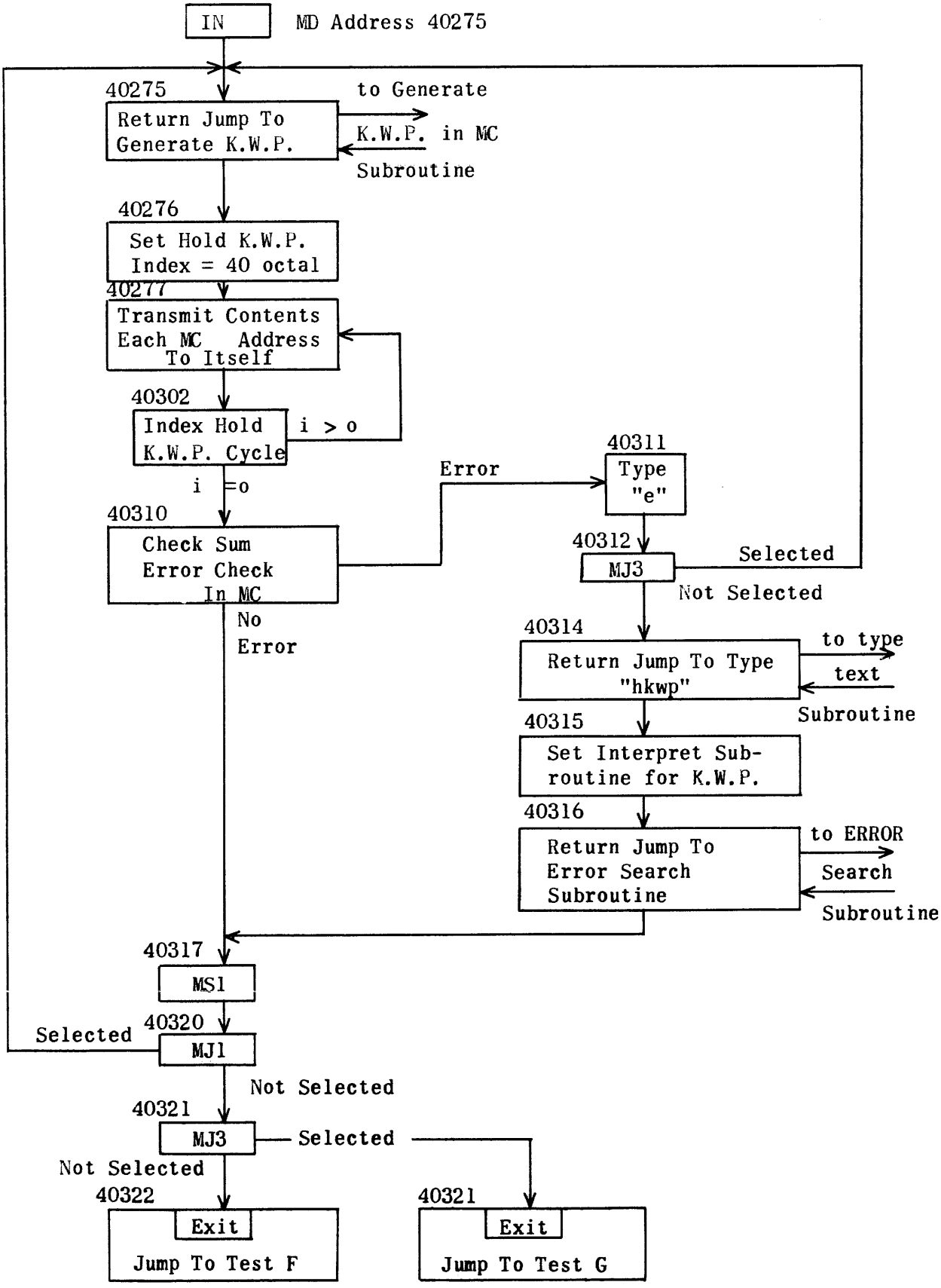


Figure 8. Test E Flow Chart of MC Test Routine
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST E
40275	37	40274	40254	Jump to generate K.W.P. in MC.
40276	11	40103	31000	Set index in Q.
40277	75	37777	40301	Read and Write contents of each MC address to itself.
40300	11	00000	00000	
40301	11	07777	07777	
40302	41	31000	40277	Perform cycle 32 times.
40303	23	31000	31000	Clear Q and A.
40304	75	27777	40306	Sum MC contents in A, and shift A left 61 places.
40305	32	00000	00000	
40306	32	07777	00075	
40307	34	40104	00000	Subtract correct check sum from A.
40310	47	40311	40317	Check for error. If A $\neq$ 0, test e failed. Type "e hkwp" (on Short MC Test type e)and repeat Test E. If A = 0, continue the test.
40311	61	00000	40254	Type "e".
40312	45	30000	40275	If Test E fails, repeat Test E on Short MC Test.
40313	11	40323	31000	Set type text subroutine parameters for "hkwp".
40314	37	41512	41501	Jump to type text subroutine to type out "hkwp".
40315	16	41500	41343	Transmit type text subroutine parameter to Q.
40316	37	41151	41104	Jump to error search subroutine.
40317	56	10000	40320	Stop after Test E if MS1 is selected.
40320	45	10000	40275	Repeat Test E if MJ1 is selected.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40321	45	30000	40357	Jump to Test G on Short MC Test.
40322	45	00000	40325	Jump to Test F.
40323	00	40324	00000	Type text subroutine parameter for "hkwp".
40324	04	05363	11545	Flex type out code for "hkwp".

TEST F. CIRCULATE WORST PATTERN

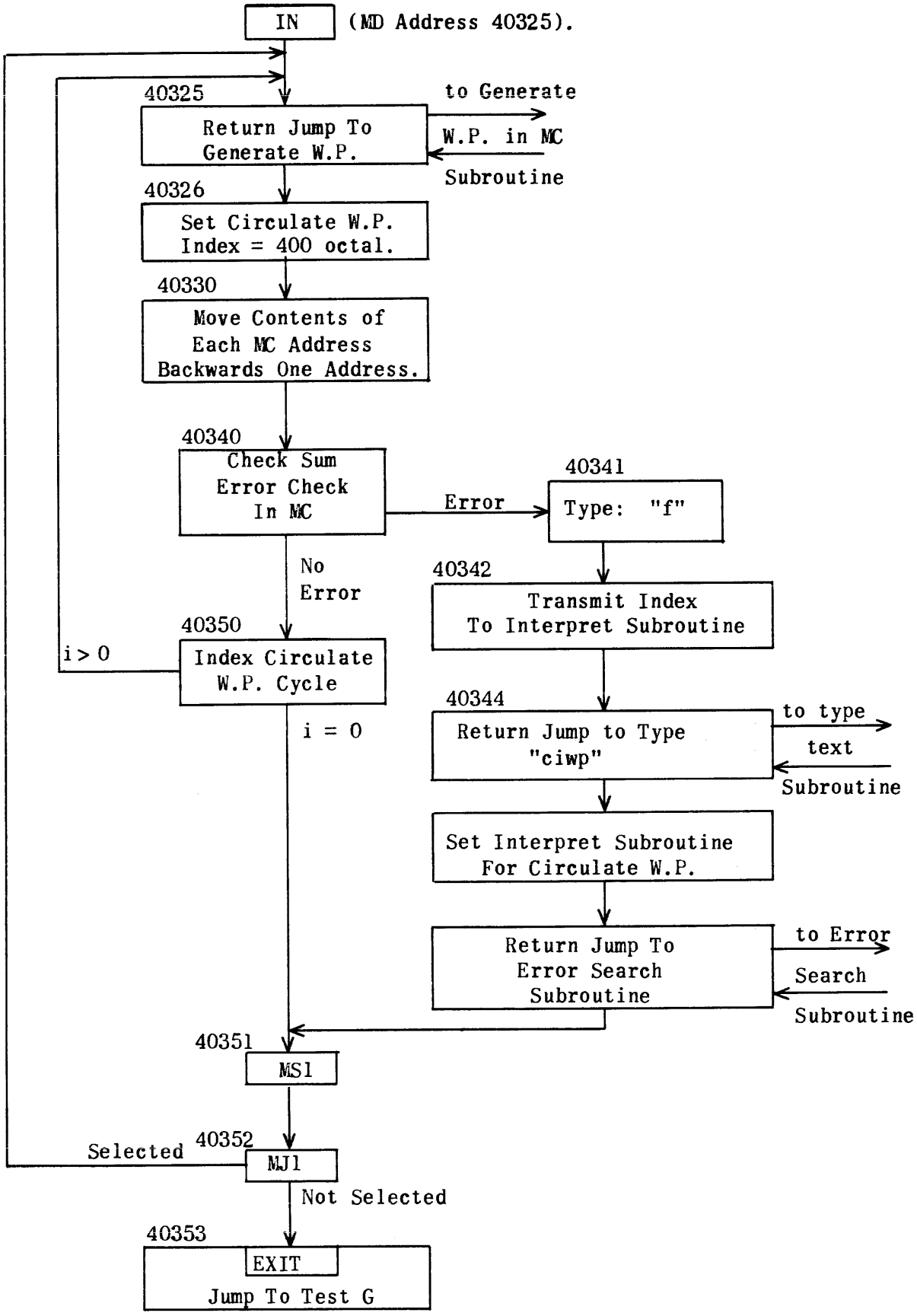


Figure 9. Test F Flow Chart of MC Test Routine
PX 142

TABLE 3. MC TEST ROUTINES (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST F
40325	37	40224	40204	Jump to generate W.P. in MC.
40326	11	40354	31026	Set index in Q.
40327	31	00000	00000	Transmit contents of MC address 00000 to A.
40330	75	37777	40332	Circulate contents of MC addresses 00001 thru 07777 backward 1 address.
40331	11	00001	00000	
40332	11	32000	07777	Transmit (A) to MC address 07777.
40333	23	32000	32000	Clear A
40334	75	27777	40336	Sum MC contents in A, and shift A left 61 places.
40335	32	00000	00000	
40336	32	07777	00075	
40337	34	40104	00000	Subtract correct check sum from A.
40340	47	40341	40350	Check for error. If A $\neq$ 0, test f failed. Type "f ciwp". If A = 0, continue the test.
40341	61	00000	40326	Type "f".
40342	11	31000	41437	Transmit remainder of index to interpret subroutine.
40343	11	40355	31000	Transmit type text subroutine parameter to Q.
40344	37	41512	41501	Jump to type text subroutine to type "ciwp".
40345	16	41477	41343	Prepare interpret subroutine to search for ciwp errors.
40346	37	41151	41104	Jump to error search subroutine.
40347	45	00000	40351	Jump to terminate Test F.
40350	41	31000	40327	Perform circulate pattern cycle 400 octal times.
40351	56	10000	40352	Stop after Test F if MS1 is selected.
40352	45	10000	40325	Repeat Test F if MJ1 is selected.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40353	45	00000	40357	Jump to Test G.
40354	00	00000	00377	Index for circulate worst pattern.
40355	00	40356	00000	Type text subroutine parameter for "ciwp".
40356	04	16143	11545	Flex type out code for "ciwp".

MAGNETIC CORE STORAGE TEST

TEST G. CROSS TALK WORST PATTERN (C.T.W.P.)

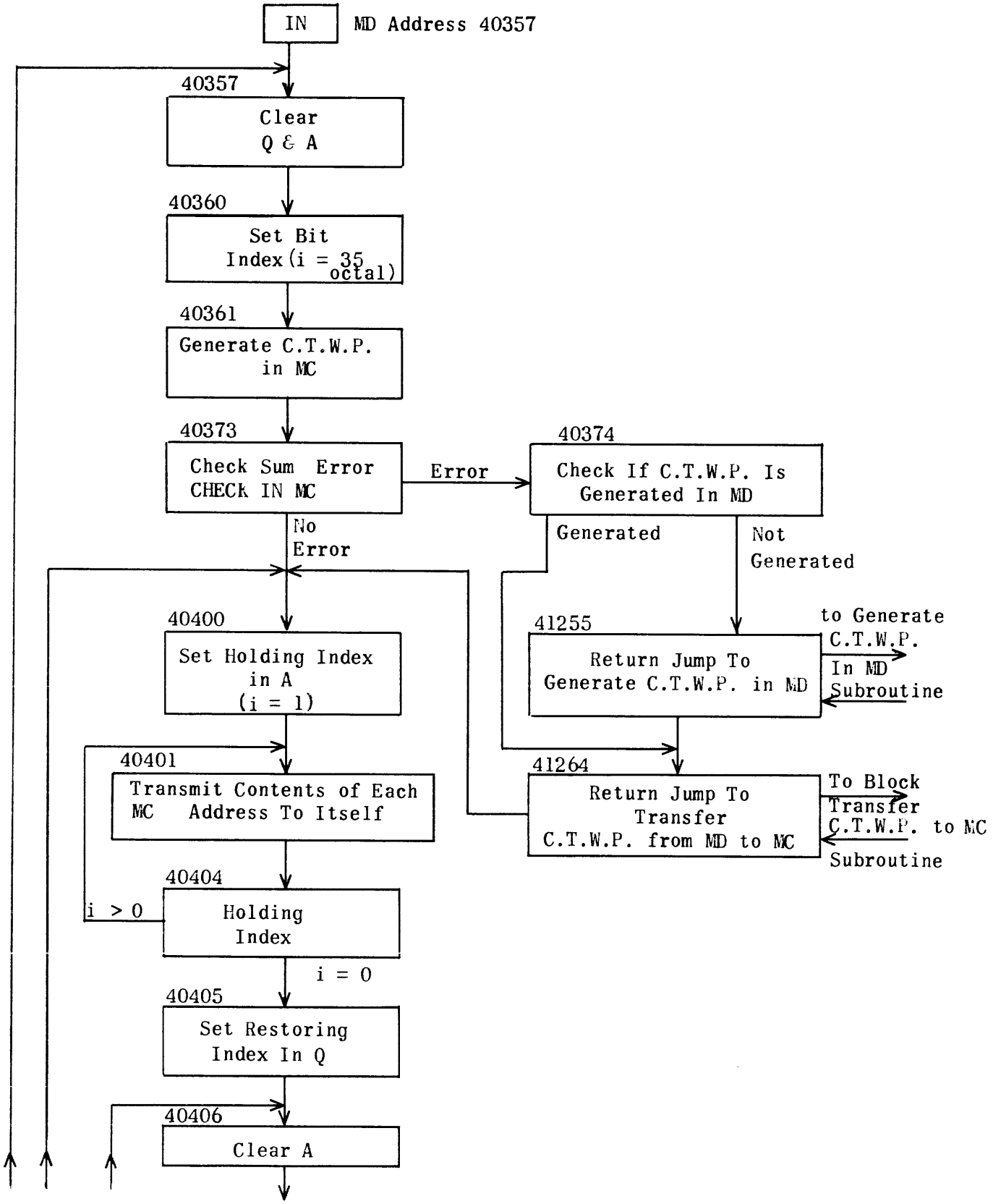


Figure 10. Test G Flow Chart Of MC Test Routine
PX 142

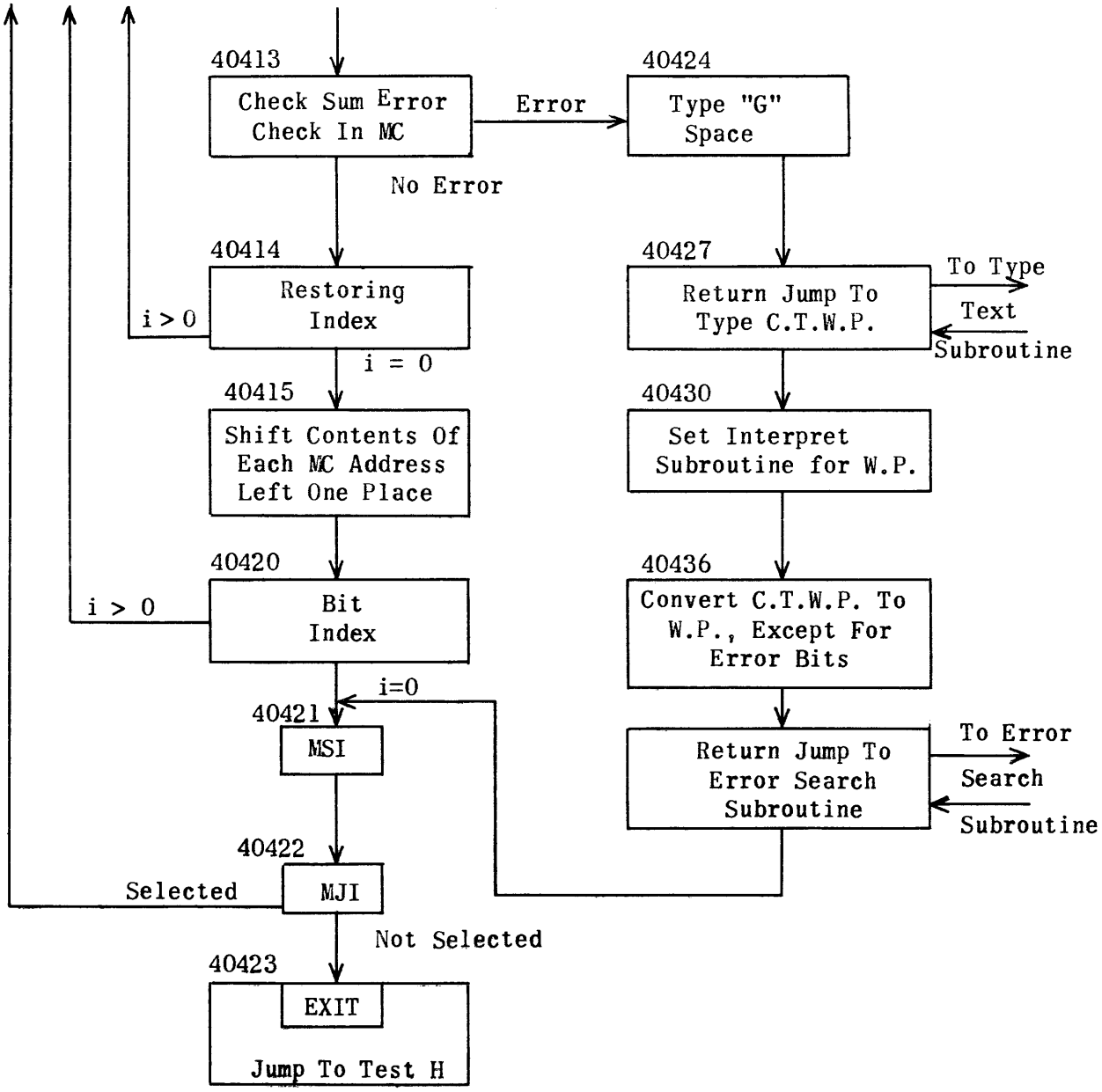


Figure 10. Test G Flow Chart Of MC Test Routine (Cont.)
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST G
40357	23	31000	31000	Clear Q and A.
40360	11	40444	40445	Set bit index to 35 for shifting pattern.
40361	11	40443	00000	Generate crosstalk worst pattern (C.T.W.P.) in MC.
40362	13	00000	00001	
40363	75	30176	40365	
40364	13	00000	00002	
40365	75	37600	40367	
40366	13	00000	00200	
40367	75	27777	40371	Sum MC contents in A and shift A left 61 places.
40370	32	00000	00000	
40371	32	07777	00075	
40372	34	40104	00000	Subtract correct check sum from A.
40373	47	40374	40400	Check for error. If A ≠ 0, C.T.W.P. has not been generated correctly in MC. Jump to generate C.T.W.P. in MD. If A = 0, continue the test.
40374	11	40032	31000	Check if C.T.W.P. is generated in MD. If C.T.W.P. is in MD, jump to transfer C.T.W.P. to MC; if not, jump to generate C.T.W.P. in MD.
40375	44	40377	40376	
40376	37	41264	41255	
40377	45	00000	41307	
40400	11	40443	32013	Set index in A for holding pattern.
40401	75	37777	40403	Read and write contents of each MC address to itself.
40402	11	00000	00000	
40403	11	07777	07777	
40404	41	32000	40401	Repeat hold cycle two times.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40405	11	40443	31000	Set index for restoring pattern.
40406	23	32000	32000	Clear A.
40407	75	27777	40411	Sum MC contents in A and shift A left 61 places.
40410	32	00000	00000	
40411	32	07777	00075	
40412	34	40104	00000	Subtract correct check sum from A.
40413	47	40428	40414	Check for error. If A $\neq$ 0, test G failed. Type "g ctwp" (on Short MC Test type g, and repeat Test G). If A $\neq$ 0, continue the test.
40414	41	31000	40406	Repeat restore cycle two times.
40415	75	27777	40417	Left shift contents of each MC address one place.
40416	55	00000	00001	
40417	55	07777	00001	
40420	41	40445	40400	Perform instructions 40400 through 40420 inclusive, 36 times.
40421	56	10000	40422	Stop if MS1 is selected.
40422	45	10000	40357	Jump to repeat Test G if MJ1 is selected.
40423	45	00000	40450	Jump to Test H.
40424	61	00000	40400	Type "g".
40425	45	30000	40357	If Test G fails, repeat Test G on Short MC Test.
40426	11	40446	31000	Transmit type text subroutine parameter to Q.
40427	37	41512	41501	Jump to type text subroutine to type "ctwp".
40430	16	41476	41343	Set interpret subroutine to search for W.P. error bits.
40431	11	40443	31000	Transmit test word to Q.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40432	11	40444	32000	Transmit original index to A.
40433	36	40445	32000	Subtract working index from A to determine position of complemented bit.
40434	16	32000	40435	Transmit complemented bit position to v-portion of MD address 40435.
40435	55	31000	00000	Shift pattern word to working position.
40436	75	27777	40440	Convert C.T.W.P to W.P, except for error bits.
40437	27	00000	31000	
40440	27	07777	31000	
40441	37	41151	41104	Jump to Error Search Subroutine.
40442	45	00000	40421	Jump to end Test G.
40443	00	00000	00001	Pattern word (W)
40444	00	00000	00043	Index for shifting pattern.
40445	00	00000	00000	Working index storage location for shifting pattern.
40446	00	40447	00000	Type text subroutine parameter for "ctwp".
40447	04	16013	11545	Flex type out code for "ctwp".

MAGNETIC CORE STORAGE TEST

TEST H. COMPLEMENT CROSS TALK WORST PATTERN (K.C.T.W.P.)

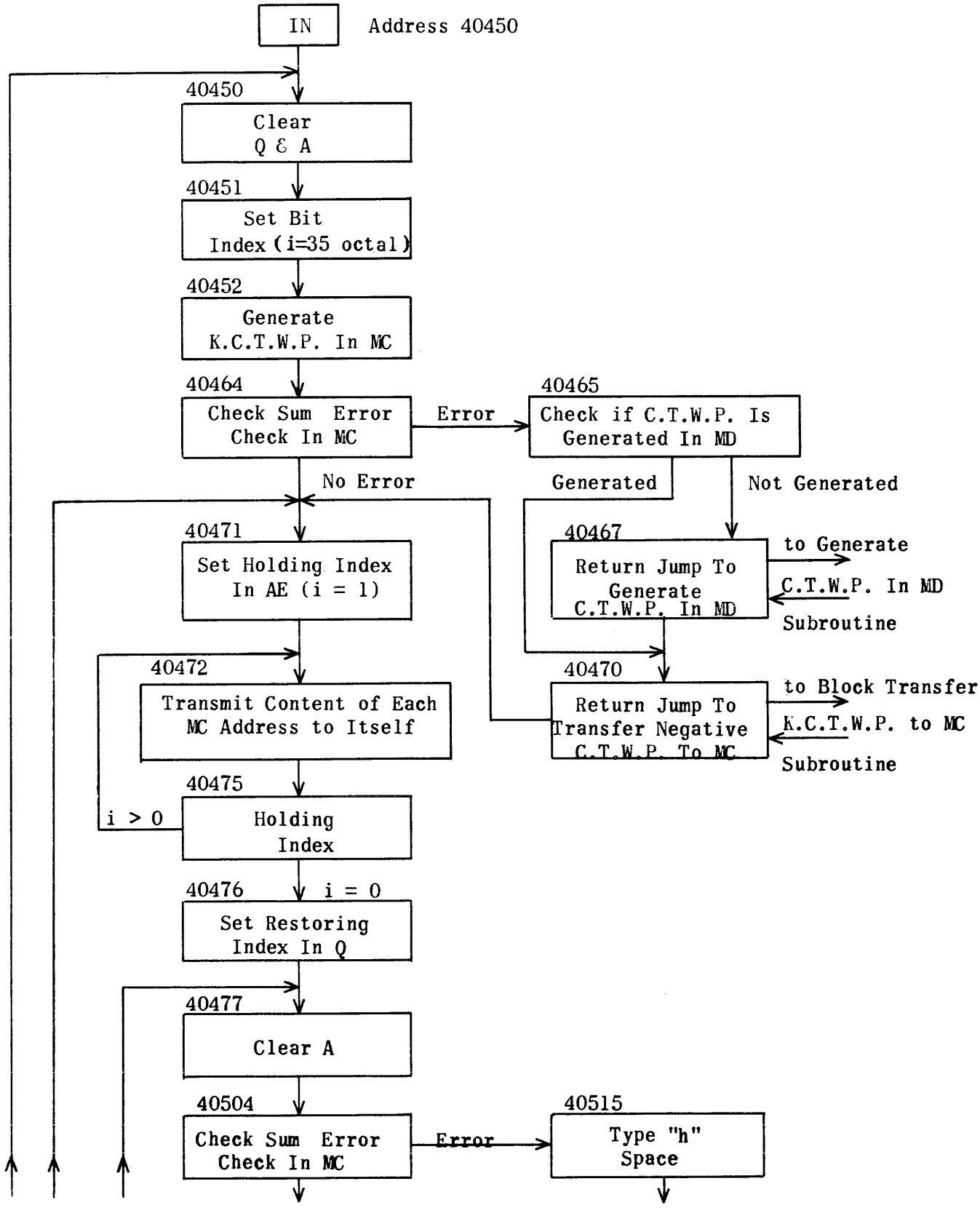


Figure 11. Test H Flow Chart Of MC Test Routine
PX 142

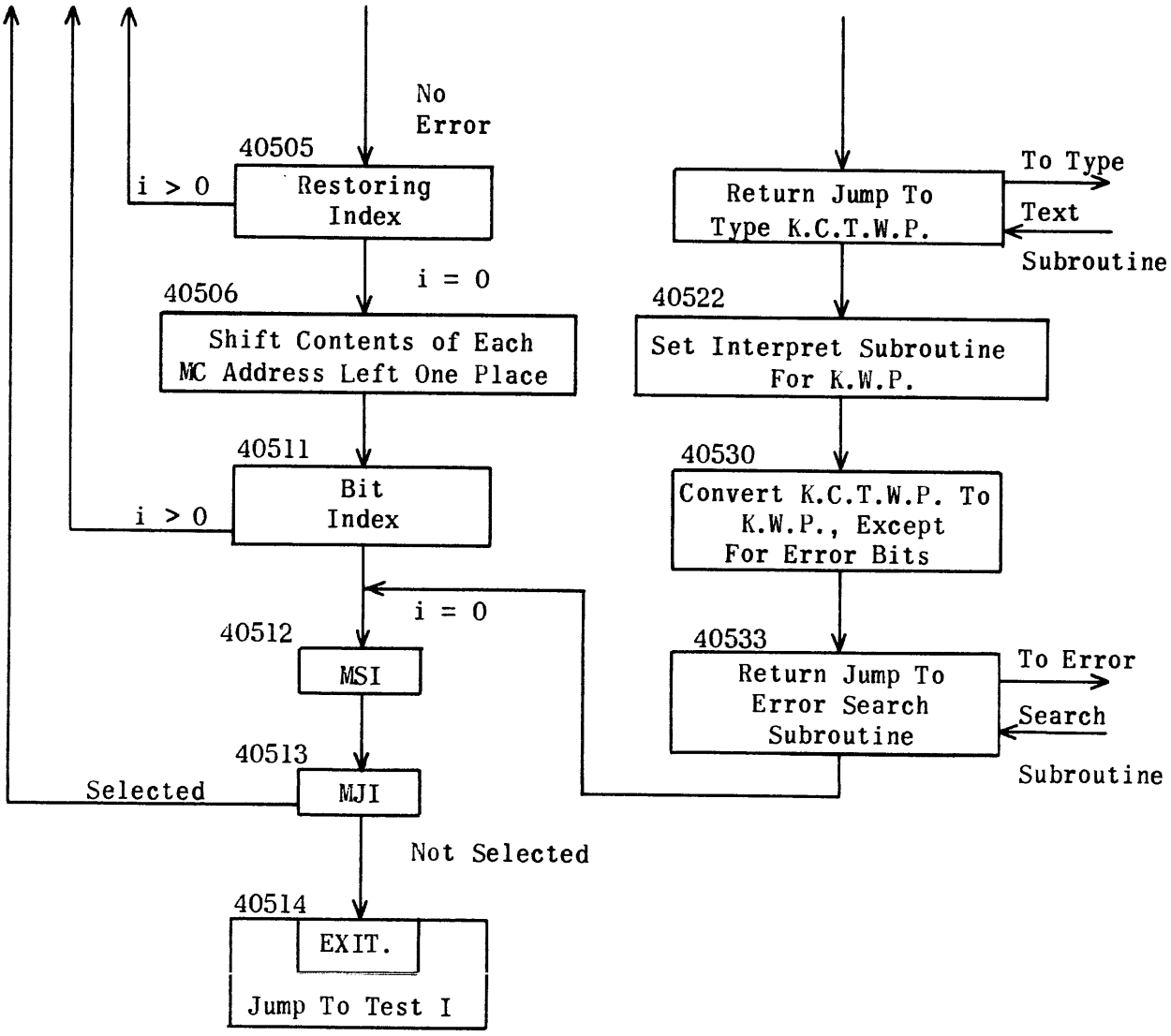


Figure 11. Test H Flow Chart Of MC Test Routine (Cont.)
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST H
40450	23	31000	31000	Clear Q and A.
40451	11	40444	40445	Set index to 35 for shifting pattern.
40452	13	40443	00000	Generate complement crosstalk worst pattern (K.C.T.W.P.) in MC.
40453	13	00000	00001	
40454	75	30176	40456	
40455	13	00000	00002	
40456	75	37600	40460	
40457	13	00000	00200	
40460	75	27777	40462	Sum MC contents in A, and shift A left 61 places.
40461	32	00000	00000	
40462	32	07777	00075	
40463	34	40104	00000	Subtract correct check sum from A.
40464	47	40465	40471	Check for error. If A $\neq$ 0, K.C.T.W.P. has not been generated in MC correctly. Jump to generate K.C.T.W.P. in MD. If A = 0, continue the test.
40465	11	40032	31004	Check if K.C.T.W.P. is generated in MD. If K.C.T.W.P. is in MD, jump to transfer K.C.T.W.P. to MC. If K.C.T.W.P. is not in MD, jump to generate K.C.T.W.P. in MD.
40466	44	40470	40467	
40467	37	41264	41255	
40470	45	00000	41320	
40471	11	40443	32005	Set index in A. for holding pattern.
40472	75	37777	40474	Read and write contents of each MC address to itself.
40473	11	00000	00000	
40474	11	07777	07777	
40475	41	32000	40472	Repeat hold cycle two times.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40476	11	40443	31000	Set index for restoring pattern.
40477	23	32000	32000	Clear A.
40500	75	27777	40502	Sum MC contents in A, and shift A left 61 places.
40501	32	00000	00000	
40502	32	07777	00075	
40503	34	40104	00000	Subtract correct check sum from A.
40504	47	40515	40505	Check for error. If A ≠ 0, test H failed. Type "h kctwp" (on Short MC Test type "h", and repeat test H.) If A = 0, continue the test.
40505	41	31000	40477	Repeat restore cycle two times.
40506	75	27777	40510	Left shift contents of each MC address one place.
40507	55	00000	00001	
40510	55	07777	00001	
40511	41	40445	40471	Perform instructions 40471 through 40511, inclusive, 36 times.
40512	56	10000	40513	Stop if MS1 is selected.
40513	45	10000	40450	Jump to repeat Test H if MS1 is selected.
40514	45	00000	40540	Jump to Test I.
40515	61	00000	40471	Type "h".
40516	45	30000	40450	If Test A fails, repeat Test H on Short MC Test.
40517	61	00000	40465	Type space.
40520	11	40535	31000	Transmit type text subroutine parameter to Q.
40521	37	41512	41501	Jump to type text subroutine to type "kctwp"
40522	16	41500	41343	Set interpret subroutine to search for K.W.P. error bits.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40523	11	40443	31000	Transmit pattern word to Q.
40524	11	40444	32000	Transmit original index to A.
40525	36	40445	32000	Subtract working index from A to determine position of complemented bit.
40526	16	32000	40527	Transmit complemented bit position to MD address 40526.
40527	55	31000	00000	Shift pattern word to working position.
40530	75	27777	40532	Convert K.C.T.W.P. to K.W.P., except for error bits.
40531	27	00000	31000	
40532	27	07777	31000	
40533	37	41151	41104	Jump to error search subroutine.
40534	45	00000	40512	Jump to end Test H.
40535	00	40536	00000	Type text subroutine parameter for "kctwp".
40536	36	16013	11545	Flex type out code for "kctwp".
40537	25	25252	52525	Test word for Test K.

MAGNETIC CORE STORAGE TEST

TEST I. INHIBIT DISTURB SENSITIVITY

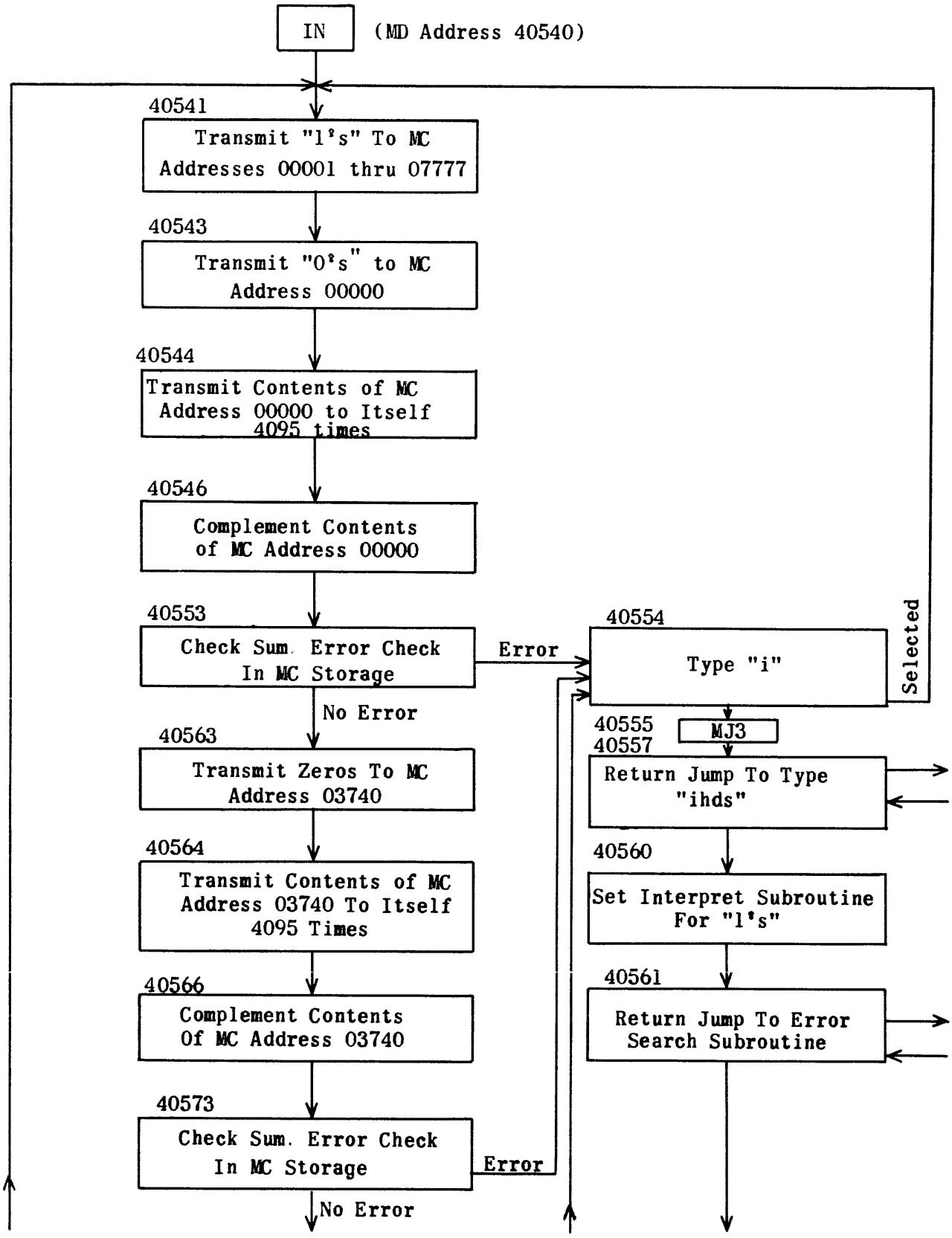


Figure 12. Test I Flow Chart of MC Test Routine
PX 142

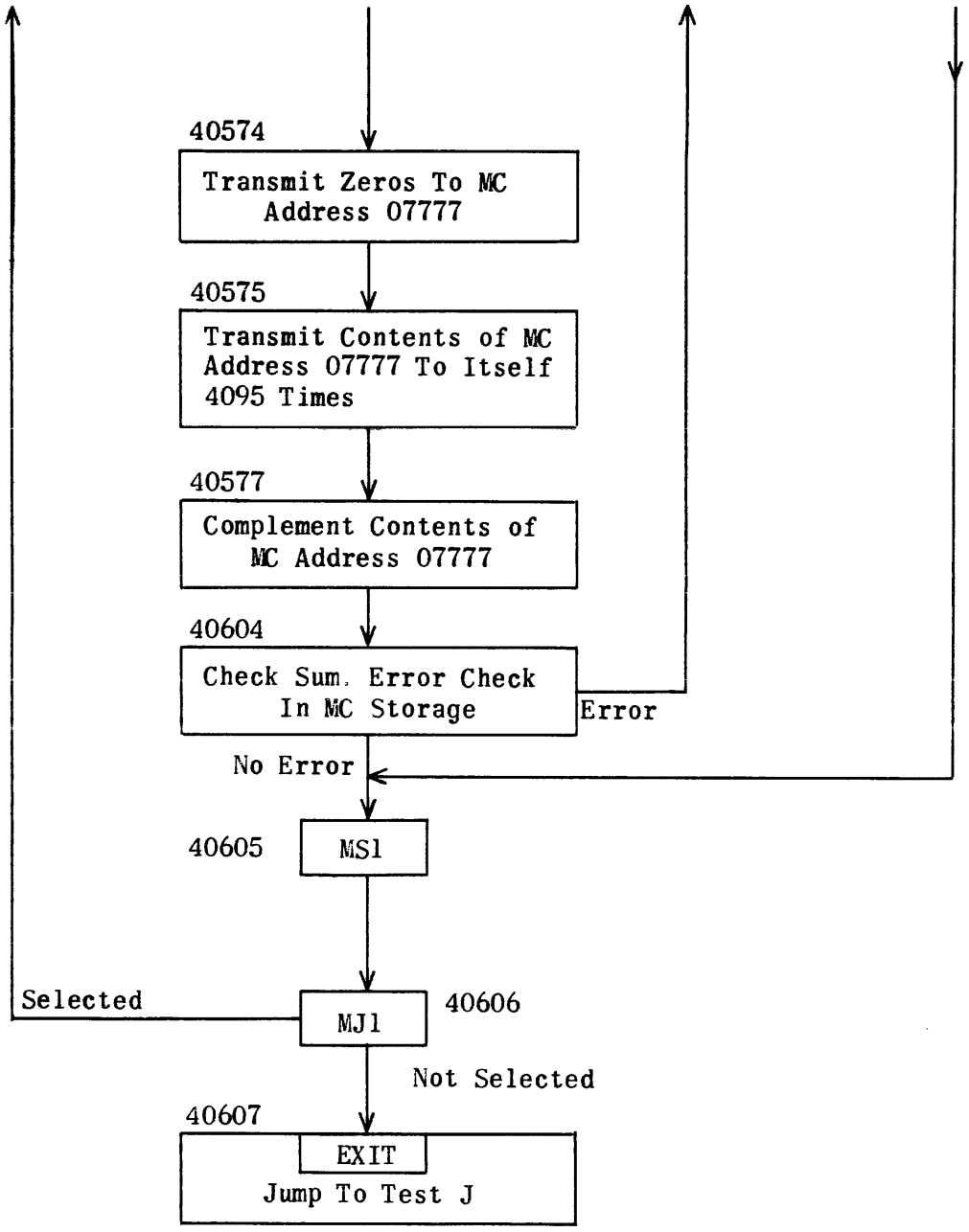


Figure 12. Test I of MC Test Routine Flow Chart (Cont.)
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST I
40540	23	31000	31014	Clear Q and A.
40541	75	17777	40543	Transmit "1's" to MC addresses 00001 thru 07777.
40542	13	31000	00001	
40543	11	31000	00000	Transmit "0's" to address 00000.
40544	75	07777	40546	Transmit contents of MC address 00000 to itself 7777 octal times.
40545	11	00000	00000	
40546	13	00000	00000	Complement MC address 00000.
40547	75	27777	40557	Sum MC contents in A, and shift A left 60 places.
40550	32	00000	00000	
40551	32	07777	00074	
40552	34	40104	00000	Subtract the correct check sum from A.
40553	47	40554	40563	Check for error. If A $\neq$ 0, test i failed. Type "i ihds" (on Short MC Test type g, and repeat Test I). If A = 0, proceed to the second part of test i.
40554	61	00000	40540	Type "i".
40555	45	30000	40540	If Test I fails, repeat Test I on Short MC Test.
40556	11	40610	31000	Transmit type text subroutine parameter to Q.
40557	37	41512	41501	Jump to type text subroutine, and type "ihds".
40560	16	41475	41343	Set interpret subroutine for all "1's".
40561	37	41151	41104	Jump to error search subroutine.
40562	45	00000	40605	Jump to end Test I.
40563	11	31000	03740	Transmit "0's" to MC address 3740.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40564	75	07777	40566	Transmit contents of MC address 3740 to itself 7777 octal times.
40565	11	03740	03740	
40566	13	03740	03740	Complement contents of MC address 3740.
40567	75	27777	40571	Sum MC contents in A, and shift A left 60 places.
40570	32	00000	00000	
40571	32	07777	00074	
40572	34	40104	00000	Subtract the correct check sum from A.
40573	47	40554	40574	Check for error. If A ≠ 0, the second part of test i failed. Type "i ihds" (on Short MC Test type "i", and repeat Test I); if A = 0, proceed to the third part of test i.
40574	11	31000	07777	Transmit "0's" to MC address 07777.
40575	75	07777	40577	Transmit contents of MC address 07777 to itself 7777 octal times.
40576	11	07777	07777	
40577	13	07777	07777	Complement MC address 07777.
40600	75	27777	40602	Sum MC contents in A and shift A left 60 places.
40601	32	00000	00000	
40602	32	07777	00074	
40603	34	40104	00000	Subtract the correct check sum from A.
40604	47	40554	40604	Check for error. If A ≠ 0, the third part of test i failed. Type "i ihds" (on Short MC Test type i, and repeat Test I). If A = 0, jump to end Test I.
40605	56	10000	40606	Stop after Test I if MS1 is selected.
40606	45	10000	40540	Repeat Test I if MJ1 is selected.
40607	45	00000	40612	Jump to Test J.
40610	00	40611	00000	Type text subroutine parameter for "ihds".
40611	04	14052	22445	Flex typeout code for "ihds".

MAGNETIC CORE STORAGE TEST

TEST J. WINDOW SHADE TEST

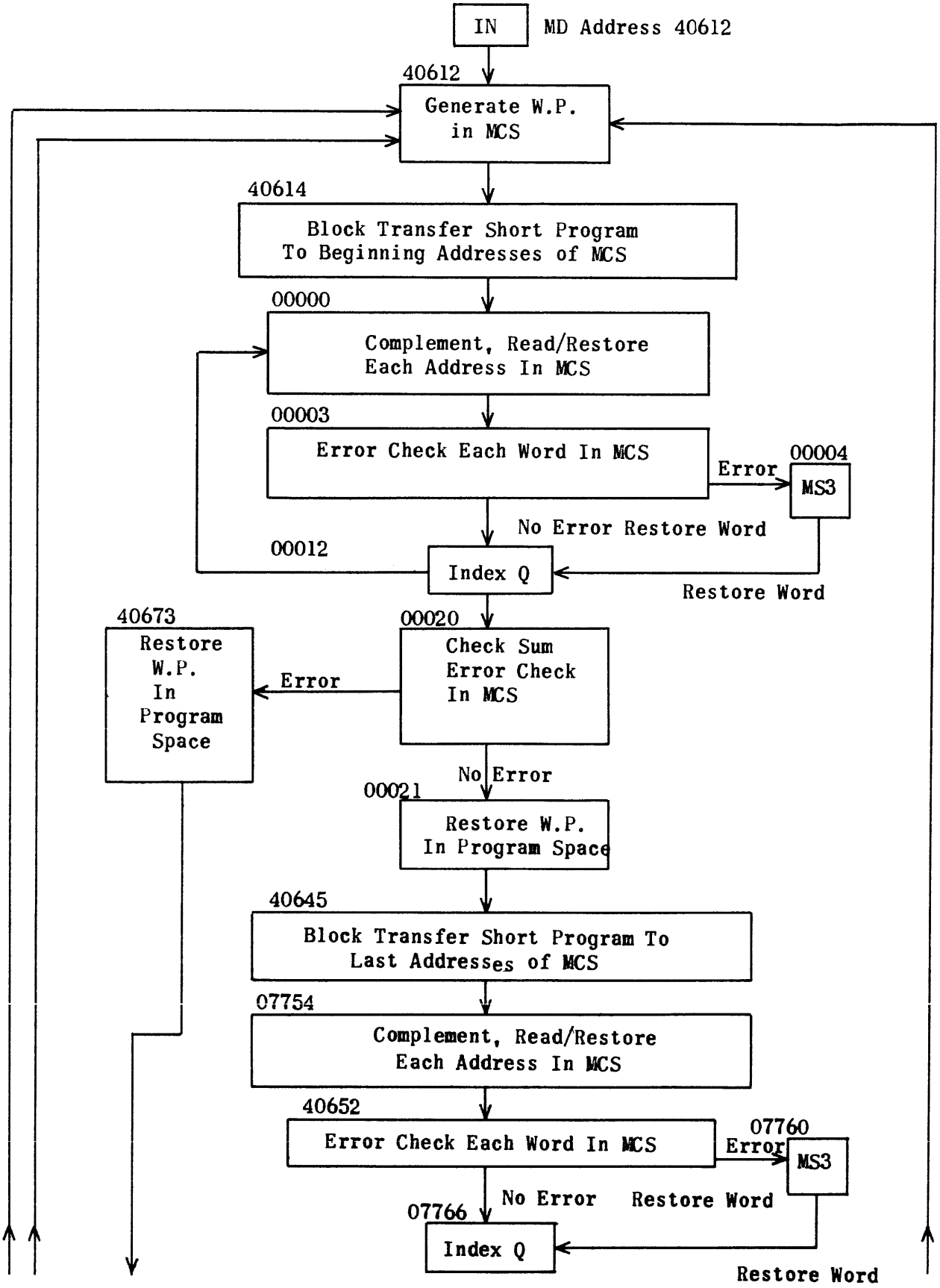


Figure 13. Test J Flow Chart of MC Test Routine
PX 142

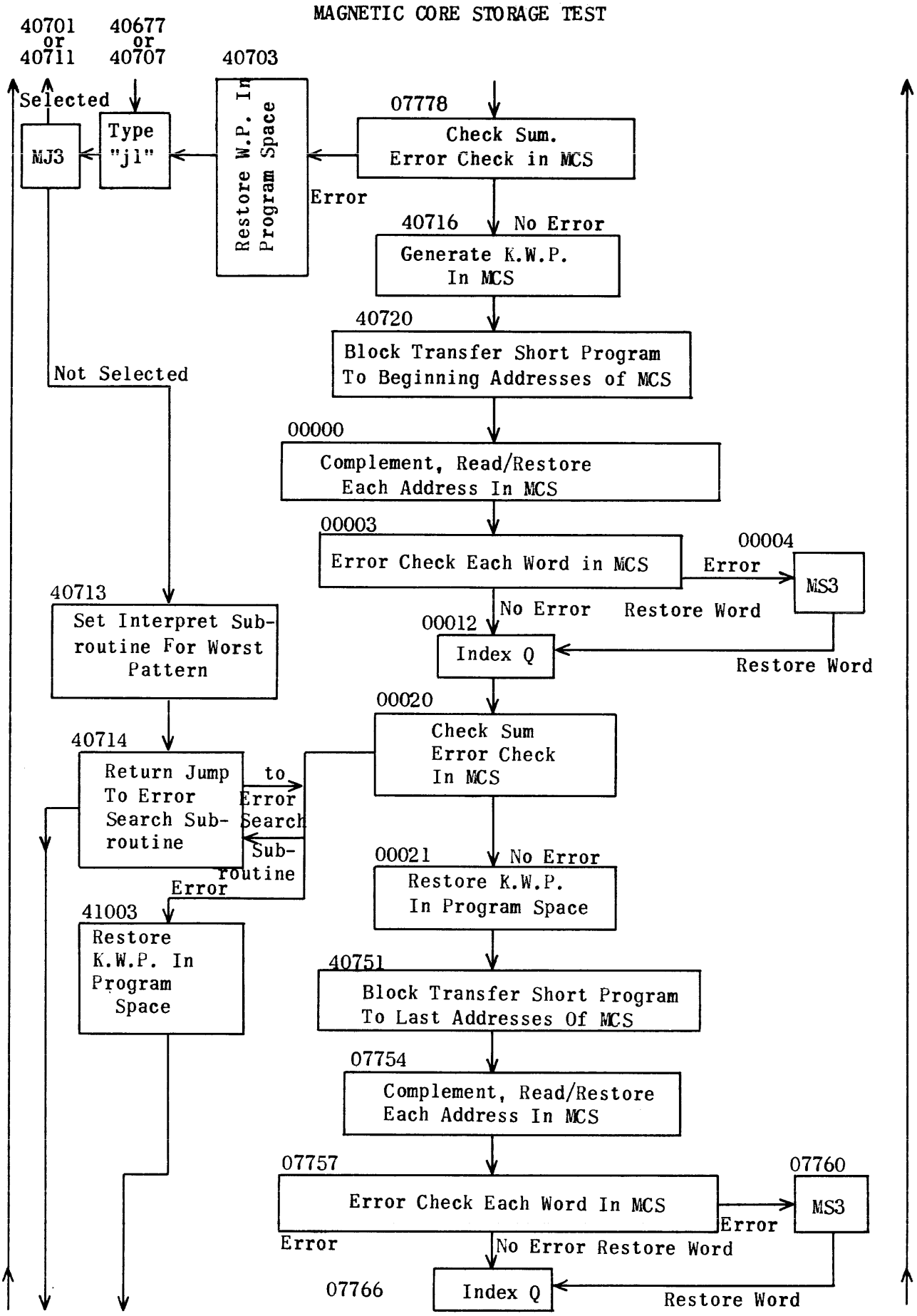
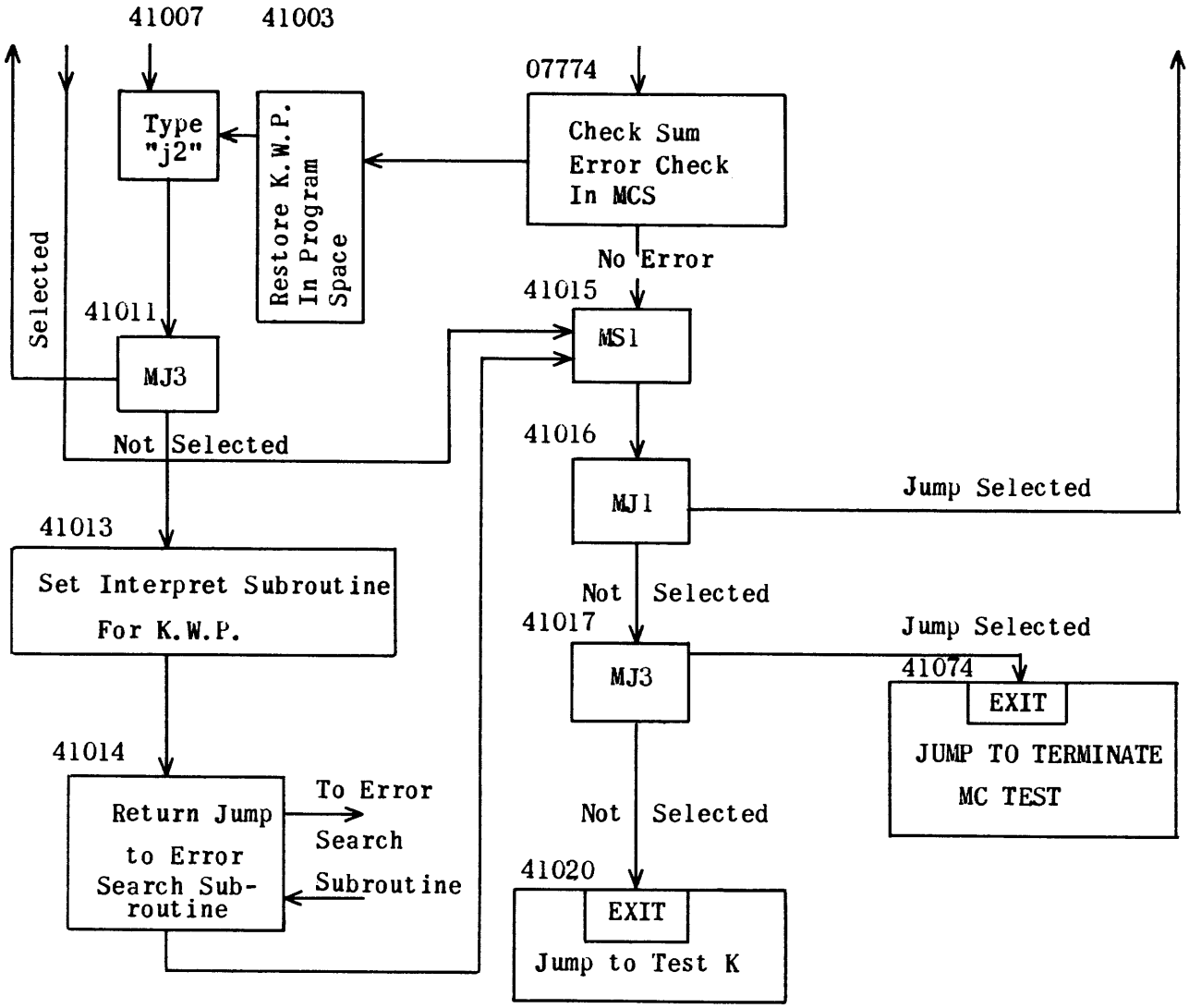


Figure 13. Test J Flow Chart of MC Test Routine (Cont.)
PX 142



MS3. - Stop after failure to restore any word in presence of worst pattern or complement worst pattern.

Figure 13. Test J Flow Chart of MC Test Routine (Cont.)
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST J
40612	37	40224	40204	Jump to generate W.P. in MC.
40613	11	41021	31000	Set word index in Q.
40614	75	30026	00000	Transfer program to MC addresses 00000 thru 00025 inclusive, and jump to MC address 00000.
40615	11	40616	00000	
40616 thru 40643				See 00000 thru 00025
00000	13	00026	00026	Complement word in MC address. (Address changed by program.)
00001	11	00026	32000	Read and restore word in MC address.
00002	11	00026	32000	Transmit word to A.
00003	47	00004	00005	Error check. If A $\neq$ 0, an error occurred; stop if MS3 is selected, and continue test if MS3 is not selected. If A = 0, continue the test.
00004	56	30000	00005	Stop if an error occurs and MS3 is selected.
00005	13	00026	00026	Restore word.
00006	21	00000	00023	Advance program addresses by 1.
00007	15	00000	00001	
00010	15	00000	00002	
00011	11	00000	00005	
00012	41	31000	00000	Index Q. (Repeat instructions 00000 through 00011 until each MC address 00026 through 07777 has been used.)
00013	23	31000	31045	Clear Q and A.
00014	75	27752	00016	Add the contents of each MC address 00026 through 07777 to A.
00015	32	00026	00000	
00016	34	00024	00044	Subtract correct check sum from A.
00017	34	00025	00000	

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00020	47	40673	00021	Error check. If A ≠ 0, test jl failed. Type "jl" and jump to error search subroutine. If A = 0, continue the present sequence.
00021	75	30026	40644	Restore W.P. to MC addresses 00000 through 00025 and jump to MD address 40644.
00022	11	00100	00000	
00023	00	00001	00001	Advance address operand.
00024	77	77777	74013	Correct check sum operands.
00025	00	00000	03764	
40644	11	41022	31000	Set Index in Q.
40645	75	30024	07754	Transfer program to MC addresses 07754 through 07777, inclusive, and jump to MC address 07754.
40646	11	40647	07754	
40647 thru 40672				See 07754 thru 07777.
07754	13	07753	07753	Complement word in MC address. (Address changed by program.)
07755	11	07753	32032	Read and restore word in MC address.
07756	11	07753	32052	Transmit word to A.
07757	47	07760	07761	Error check. If A ≠ 0, an error has occurred. Stop if MS3 is selected, or continue test if MS3 is not selected. If A = 0, continue the test.
07760	56	30000	07761	Stop if an error occurs and MS3 is selected.
07761	13	07753	07753	Restore word.
07762	23	07754	07775	Back program addresses by 1.
07763	15	07754	07755	
07764	15	07754	07756	
07765	11	07754	07761	
07766	41	31000	07754	Index Q. (Repeat instructions 07754 through 07765 until each MC address 00000 through 07753 has been used.)

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
07767	23	31000	31074	Clear Q and A.
07770	75	27754	07772	Add the contents of each MC address 00000 through 07753 to A.
07771	32	00000	00000	
07772	34	07776	00044	Subtract correct check sum from A.
07773	34	07777	00000	
07774	47	40703	40716	If A $\neq$ 0, test j1 failed. Restore pattern in MC and type j1. If A = 0, jump to test j2.
07775	00	00001	00001	Back addresses operand.
07776	77	77777	74012	Correct check sum operands.
07777	00	00000	03765	
40673	11	31000	00000	Transmit "0's" to MC address 00000.
40674	13	31000	00001	Transmit "1's" to MC address 00001.
40675	75	30024	40677	Restore W.P. to MC addresses 00002 through 00025, inclusive.
40676	13	00000	00002	
40677	61	00000	40650	Type "j".
40700	61	00000	40651	Type "1".
40701	45	30000	40612	Repeat Test J on Short MC Test.
40702	45	00000	40712	Jump to error search preparation.
40703	13	31000	07754	Transmit "1's" to MC address 07754.
40704	11	31000	07755	Transmit "0's" to MC address 07755.
40705	75	30022	40707	Restore W.P. to MC addresses 07756 through 07777, inclusive.
40706	13	07754	07756	
40707	61	00000	40650	Type "j".
40710	61	00000	40651	Type "1".

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
40711	45	30000	40612	Repeat Test J on Short MC Test.
40712	61	00000	40631	Carriage return.
40713	16	41476	41343	Set Interpret Subroutine jump address.
40714	37	41151	41104	Jump to error search subroutine.
40715	45	00000	41015	Jump to terminate Test J.
40716	37	40274	40254	Jump to generate K.W.P. in MCS.
40717	11	41021	31032	Set word index.
40720	75	30026	00000	Transfer program to MC addresses 00000 through 00025, inclusive.
40721	11	40722	00000	
40722 thru 40747				See 00000 thru 00025
00000	13	00026	00026	Complement word in MC address.
00001	11	00026	32000	Read and restore word in MC address.
00002	11	00026	32000	Transmit word to A.
00003	47	00004	00005	Error check. If A $\neq$ 0, an error has occurred. Stop if MS3 is selected, and continue test if MS3 is not selected. If A = 0, continue the test.
00004	56	30000	00005	Stop if an error occurs and MS3 is selected.
00005	13	00026	00026	Restore word.
00006	21	00000	00023	Advance program address by 1.
00007	15	00000	00001	
00010	15	00000	00002	
00011	11	00000	00005	
00012	41	31000	00000	Index Q. (Repeat instructions 00000 through 00011 until each MC address 00026 through 07777 has been used.)
00013	23	31000	31074	Clear Q & A.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00014	75	27752	00016	Add the contents of each MC address 00026 through 07777 to A. Subtract correct check sum from A.
00015	32	00026	00000	
00016	34	00024	00044	
00017	34	00025	00000	
00020	47	40777	00021	Error check. If A ≠ 0, test j2 failed. Type "j2", and jump to error search subroutine. If A = 0, continue the present sequence.
00021	75	30026	40750	Restore K.W.P. in MC addresses 00000 through 00025, and jump to MC address 40750.
00022	11	00100	00000	
00023	00	00001	00001	Advance address operand.
00024	77	77777	74013	Correct check sum operands.
00025	00	00000	03764	
40750	11	41022	31045	Set index in Q.
40751	75	30024	07754	Transfer program to MC addresses 07754 through 07777, inclusive, and jump to MC address 07754.
40752	11	40753	07754	
40753 thru 40776				See 07754 thru 07777.
07754	13	07753	07753	Complement word in MC address. (Address changed by program.)
07755	11	07753	32000	Read and restore word in MC address.
07756	11	07753	32000	Transmit word to A.
07757	47	07760	07761	Error check. If A ≠ 0, an error has occurred. Stop if MS3 is selected, or continue if MS3 is not selected. If A = 0, continue the test.
07760	56	30000	07761	Stop if an error occurs and MS3 is selected.
07761	13	07753	07753	Restore word.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
17762	23	07754	07775	Back program address 1.
07763	15	07754	07755	
07764	15	07754	07756	
07765	11	07754	07761	
07766	41	31000	07754	Index Q. (Repeat instructions 07759 through 07765 until each MC address 00000 through 07753 has been used.)
07767	23	31000	31000	Clear Q and A.
07770	75	27754	07772	Add the contents of each MC address, 00000 through 07753, to A. Subtract correct check sum from A.
07771	32	00000	00000	
07772	34	00776	00044	
07773	34	07777	00000	
07774	47	41003	41015	Error check. If A $\neq$ 0, test j2 failed. Type j2, and jump to error search subroutine. If A = 0, jump to end test.
07775	00	00001	00001	Back program addresses operand.
07776	77	77777	74012	Correct check sum operands.
07777	00	00000	03765	
40777	13	31000	00000	Transmit "1's" to MC address 00000.
41000	11	31000	00001	Transmit "0's" to MC address 00001.
41001	75	30024	41007	Restore K.W.P. to MC addresses 00002 through 00025, inclusive.
41002	13	00000	00002	
41003	11	31000	07754	Transmit "0's" to MC address 07754.
41004	13	31000	07755	Transmit "1's" to MC address 07755.
41005	75	30022	41007	Restore K.W.P. to MC addresses 07754 through 07777, inclusive.
41006	13	07754	07756	

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TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41007	61	00000	40717	Type "j".
41010	61	00000	40735	Type "2".
41011	45	30000	40612	Repeat Test J on Short MC Test.
41012	61	00000	40750	Carriage return.
41013	16	41500	41343	Set Interpret Subroutine jump address.
41014	37	41151	41104	Jump to Error Search Subroutine.
41015	56	10000	41016	Stop at end of Test J if MS1 is selected.
41016	45	10000	40612	Repeat Test J if MJ1 is selected.
41017	45	30000	41074	Bypass Test K on Short MC Test if MJ3 is selected.
41020	45	00000	41023	Jump to Test K.
41021	00	00000	07751	Word in index operands.
41022	00	00000	07753	

MAGNETIC CORE STORAGE TEST

TEST K. PARTIAL WRITE INSTRUCTIONS 15 and 16.

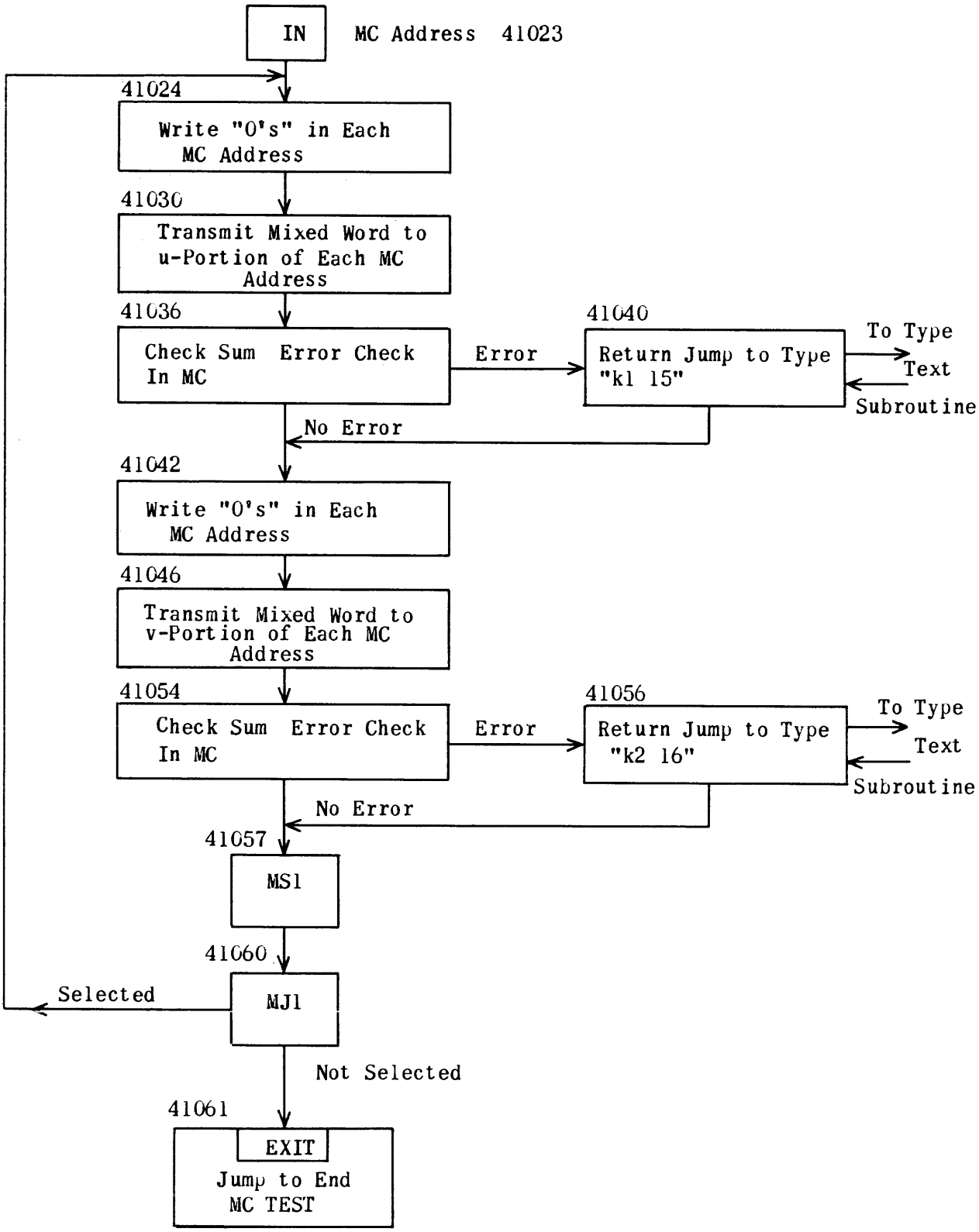

Figure 14. Test K Flow Chart of MC Test Routine
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TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TEST K.
41023	23	31000	31000	Clear Q and A.
41024	75	17777	41026	Write "0's" in each MC address.
41025	11	31000	00000	
41026	11	31000	07777	
41027	11	40537	31000	Set mixed word constant in Q.
41030	75	17777	41032	Transmit mixed word pattern to u portion of each MC address.
41031	15	31000	00000	
41032	15	31000	07777	
41033	75	27777	41035	Add the contents of each MC address to A, and shift A left 54 octal places.
41034	32	00000	00000	
41035	32	07777	00054	
41036	43	41062	41041	Error check. If A ≠ u, test k1 failed. Jump to type "k1 15". If A = u, test k1 passed, proceed to test k2.
41037	11	41063	31000	Set type parameters in Q.
41040	37	41512	41501	Jump to type "k1 15".
41041	23	31000	31000	Clear Q and A.
41042	75	17777	41044	Write "0's" in each MC address.
41043	11	31000	00000	
41044	11	31000	07777	
41045	13	40537	31000	Set mixed word constant in Q.
41046	75	17777	41050	Transmit mixed word pattern to v-portion of each MC address.
41047	16	31000	00000	
41050	16	31000	07777	

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41051	75	27777	41053	Add the contents of each MC address to A and shift A left 73 octal places.
41052	32	00000	00000	
41053	32	07777	00073	
41054	43	41062	41057	Error check. If A ≠ u, test k2 failed. Jump to type "k2 16". If A = u, proceed to end Test K.
41055	11	41065	31000	Set type parameters in Q.
41056	37	41512	41501	Jump to type"k2 16"
41057	56	10000	41060	Stop if MS1 is selected.
41060	45	10000	41023	Repeat Test K if MJ1 is selected.
41061	45	00000	41067	Jump to End MC Test Subroutine.
41062	00	00000	12525	Correct check sum operand.
41063	00	41064	00000	Type parameter for "k1 15".
41064	36	52045	26245	Type code for "k1 15".
41065	00	41066	00000	Type parameter for "k2 16".
41066	36	74045	26645	Type code for "k2 16".

MAGNETIC CORE STORAGE TEST

END TEST SUBROUTINE

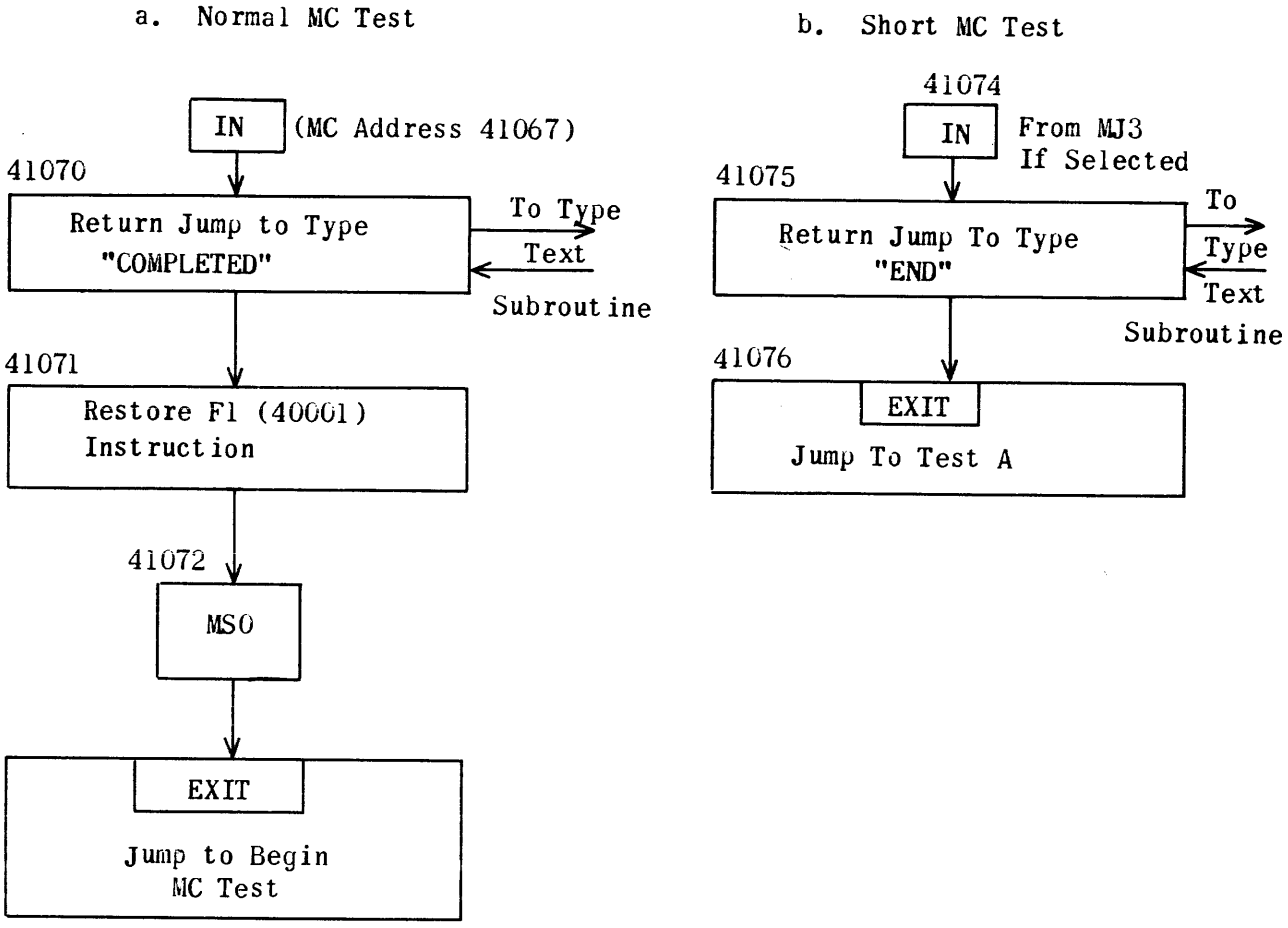

Figure 15. End Test Subroutine of MC Test Routine Flow Chart
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				END TEST SUBROUTINE
41067	11	41077	31000	Set type parameters in Q.
41070	37	41512	41501	Jump to type "COMPLETED".
41071	11	41073	40001	Restore the correct instruction address at F1.
41072	56	00000	40010	Stop. (Push start button to repeat MC Test.)
41073	45	00000	40002	Correct instruction for F1.
41074	11	41102	31000	Set type parameters in Q. (Short MC Test termination instructions.)
41075	37	41512	41501	Jump to type "END".
41076	45	00000	40033	Jump to Test A.
41077	00	41100	00001	Type parameter for "COMPLETED".
41100	04	47160	30715	Type code for "COMPLETED".
41101	11	20012	02257	
41102	00	41103	00000	Type parameter for "END".
41103	04	47200	62257	Type code for "END".

MAGNETIC CORE STORAGE TEST

ERROR SEARCH SUBROUTINE

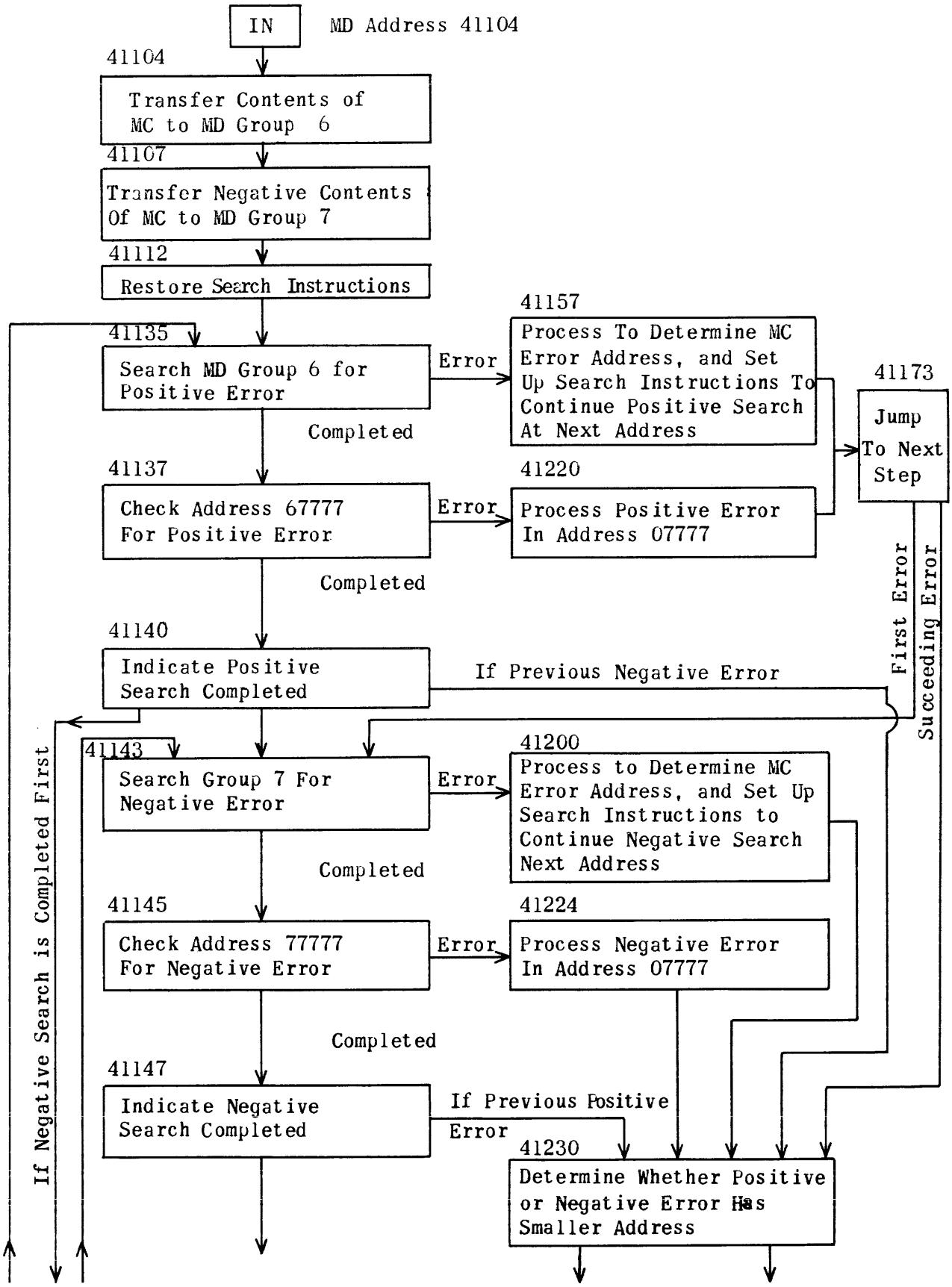

Figure 16. Error Search Subroutine Flow Chart Of MC Test Routine
PX 142

ERROR SEARCH SUBROUTINE (cont.)

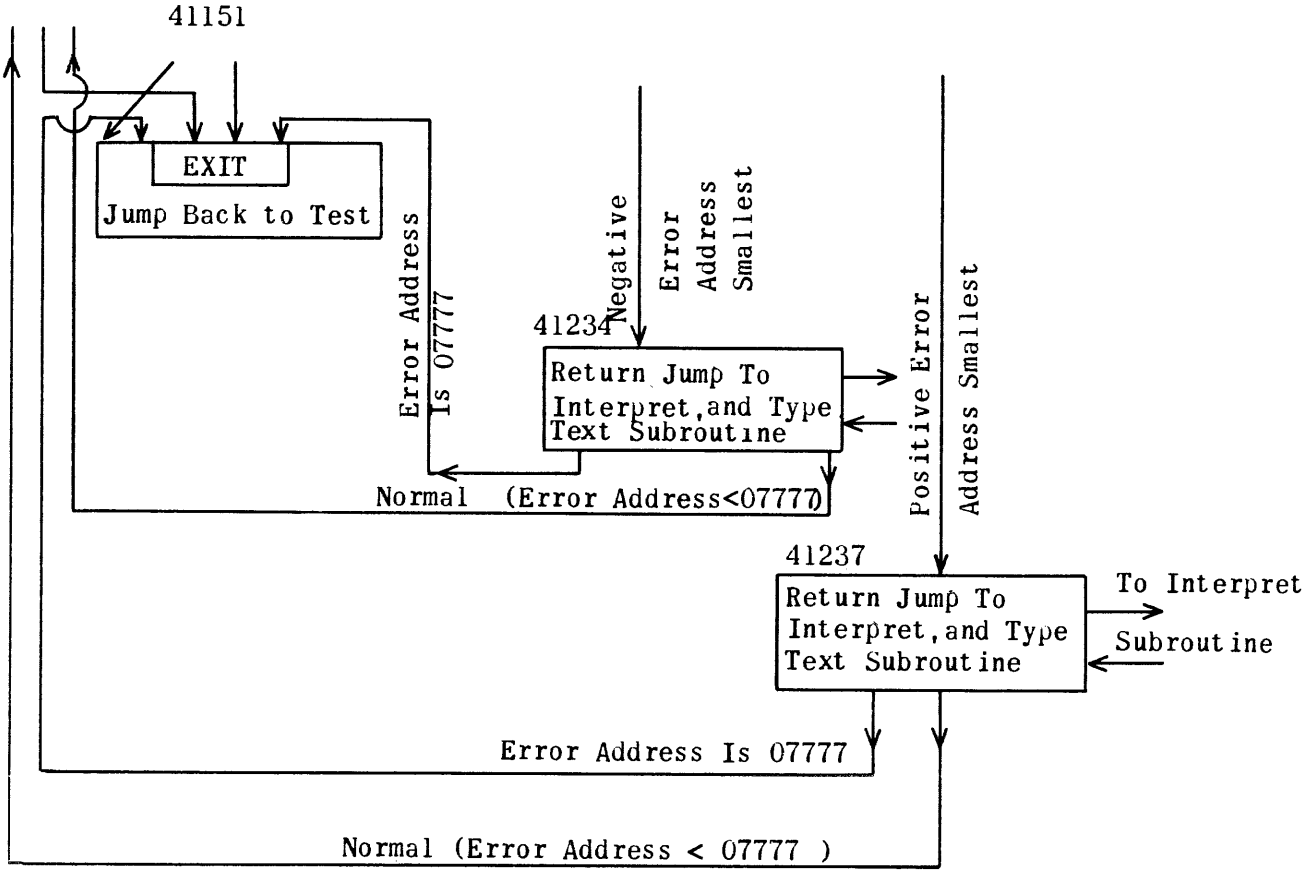

Figure 16. Error Search Subroutine Flow Chart of MC Test Routine (Cont.)
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				ERROR SEARCH SUBROUTINE
41104	75	37777	41106	Transmit contents of each MC address to Group 6 of MD.
41105	11	00000	60000	
41106	11	07777	67777	
41107	75	37777	41111	Transmit complement of contents of each MC address to Group 7 of MD.
41110	13	00000	70000	
41111	13	07777	77777	
41112	11	41126	41135	Restore error search instructions.
41113	15	41124	41136	
41114	16	41115	41142	
41115	11	41127	41143	
41116	15	41125	41144	
41117	16	41130	41150	
41120	16	41131	41173	
41121	16	41132	41214	
41122	45	00000	41134	Jump to start error search.
41123	00	00001	00000	MD error address operand.
41124	00	60000	00000	MD Group 6 starting address operand.
41125	00	70000	00000	MD Group 7 starting address operand.
41126	75	27777	41137	Original instruction stored at MD address 41135 operand.
41127	75	27777	41145	Original instruction stored at MD address 41143 operand.
41130	00	00000	41151	Original restoring operand for MD address 41150.

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TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41131	00	00000	41174	Original restoring operand for MD address 41173.
41132	00	00000	41215	Original restoring operand for MD address 41124.
41133	00	00000	07777	Last MC error address operand.
41134	23	31000	31023	Clear Q and A.
41135	75	27777	41137	Search MD Group 6 for positive error words.
41136	42	60000	41157	
41137	42	67777	41220	
41140	11	41152	41153	Set indication positive error search completed.
41141	16	41151	41150	Alter negative error search completion jump out.
41142	45	00000	41143	Jump to next step determined by progress of search.
41143	75	27777	41145	Search MD Group 7 for positive error words. (Negative originally.)
41144	42	70000	41200	
41145	42	77777	41224	
41146	16	41151	41142	Alter positive error search completion jump out address.
41147	11	41152	41155	Set indication negative error search completed.
41150	45	00000	41151	Jump to next step determined by progress of search.
41151	45	00000	00000	Jump back to test.
41152	00	00000	10000	Completion indication operand.
41153	00	00000	00000	Storage for jn and positive error address.
41154	00	00000	00000	Storage for positive error word.

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TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41155	00	00000	00000	Storage for negative error address.
41156	00	00000	00000	Storage for negative error word.
41157	55	31000	00017	Shift j (n-r) to u section of Q.
41160	11	32000	41153	Clear positive error address storage.
41161	15	41135	41153	Transmit jn to temporary storage.
41162	15	31000	41135	Transmit new jn to u-portion of positive error word search repeat instruction.
41163	23	41153	31000	Subtract j (n-r) from jn to get r (the positive error word address plus 1).
41164	35	41136	41136	Set up new repeated instruction beginning address to continue search.
41165	36	41123	32000	Subtract 1 from A to get MD error address.
41166	15	32000	41171	Transmit contents of u portion of A to error word withdrawal instruction.
41167	36	41124	32000	Change MD error address to MC error address.
41170	15	32000	41153	Store MC error address at temporary storage location.
41171	11	00000	41154	Store MC error word at temporary storage location.
41172	55	41153	00025	Shift positive MC error address to v portion of MD address 41153.
41173	45	00000	41174	Jump to next step determined by progress of search.
41174	16	41217	41150	Alter negative search completion jump out.
41175	16	41217	41173	Alter positive processing jump out.
41176	23	31000	31000	Clear Q and A.
41177	45	00000	41143	Jump to negative error search.
41200	55	31000	00017	Shift j (n-r) to u section of Q.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41201	11	32000	41155	Clear negative error address storage location.
41202	15	41143	41155	Transmit jn to temporary storage location.
41203	15	31000	41143	Transmit new jn to u portion of negative error word search repeat instruction.
41204	23	41155	31000	Subtract j (n-r) from jn to get r (the negative error word address plus 1).
41205	35	41144	41144	Set up new repeated instruction address to continue search.
41206	36	41123	32000	Subtract 1 from A to get MD error address.
41207	15	32000	41212	Transmit contents of v portion of A to error word withdrawal instruction.
41210	36	41125	32000	Change MD error address to MC error address
41211	15	32000	41155	Store MC error address at temporary storage location.
41212	13	00000	41156	Store MC error word at temporary storage location.
41213	55	41155	00025	Shift negative MC error address to v portion of MD address 41155.
41214	45	00000	41215	Jump to next step determined by the progress of the search.
41215	16	41217	41142	Alter positive search completion jump out.
41216	16	41217	41214	Alter negative processing jump out.
41217	45	00000	41230	Jump to error address comparator.
41220	11	41133	41153	Store positive error address 07777.
41221	11	67777	41154	Transfer positive MC error word at MC address 07777 to temporary storage.
41222	11	41151	41135	Alter positive search to jump back to test.
41223	45	00000	41173	Jump to next step.

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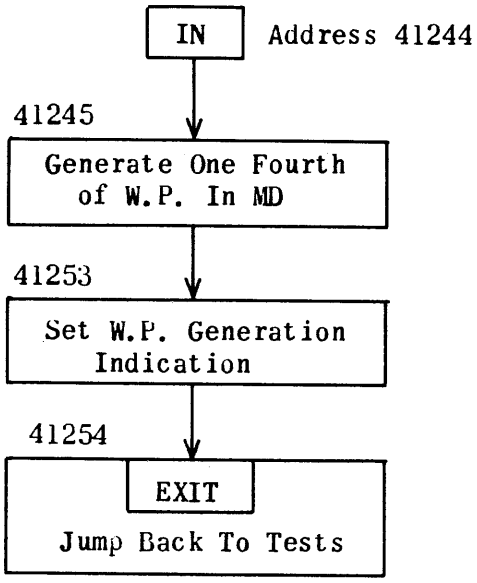
TABLE 3. MC TEST ROUTINE (Cont.)

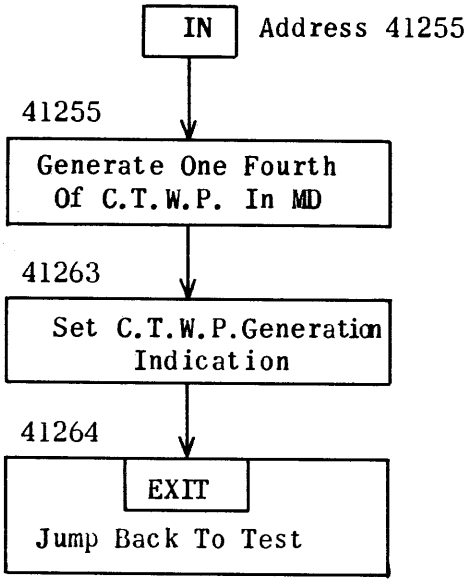
ADDRESS	OP-CODE	u	v	FUNCTION
41224	11	41133	41155	Store negative error address 07777 at temporary storage.
41225	13	77777	41156	Transfer negative MC error word at MC address to temporary storage.
41226	11	41151	41143	Alter negative search loop beginning instruction to jump back to test.
41227	45	00000	41214	Jump to next step.
41230	11	41153	32000	Transmit positive MC error address to A.
41231	42	41155	41237	Check if positive or negative MC error address is smaller.
41232	11	41155	41435	Transmit negative error address to interpret subroutine.
41233	11	41156	41436	Transmit negative error word to interpret subroutine.
41234	37	41430	41331	Jump to interpret subroutine.
41235	23	31000	31000	Clear Q and A.
41236	45	00000	41143	Jump to continue negative search.
41237	11	41153	41435	Transmit positive error address to interpret subroutine.
41240	11	41154	41436	Transmit positive error word to interpret subroutine.
41241	37	41430	41331	Jump to interpret subroutine.
41242	23	31000	31000	Clear Q and A.
41243	45	00000	41135	Jump to continue positive search.

MAGNETIC DRUM GENERATION SUBROUTINE

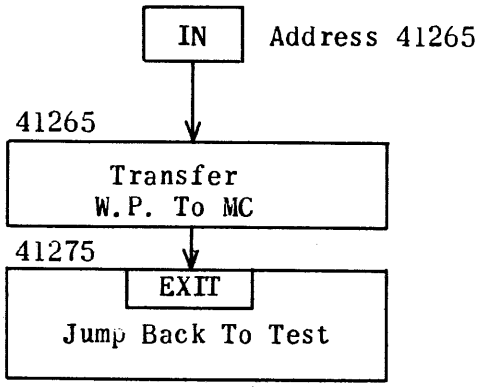
1. Generate W.P. In MD Subroutine



2. Generate C.T.W.P. in MD Subroutine



3. Transfer W.P. to MC Subroutine



4. Transfer K.W.P. to MC Subroutine

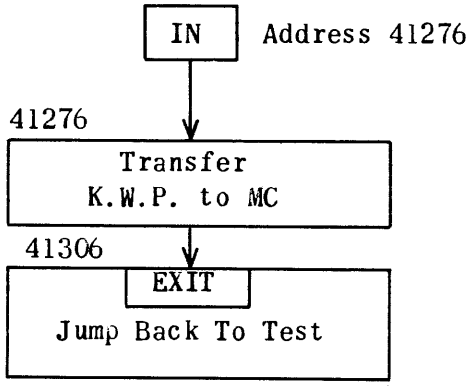


Figure 17. Magnetic Drum Generation Subroutine Flow Charts of MC Test Routine
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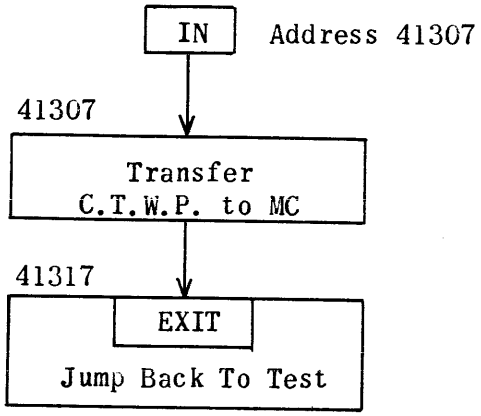
5. Transfer C.T.W.P. To MC Subroutine



6. Transfer K.C.T.W.P. To MC Subroutine

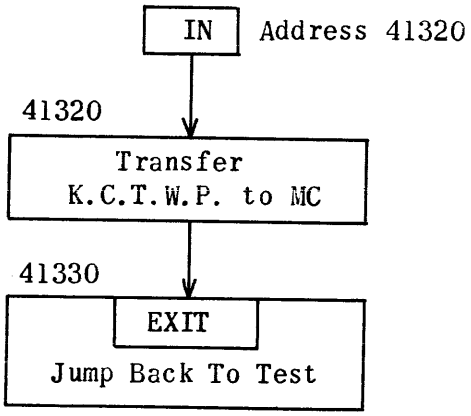


Figure 17. Magnetic Drum Generation Subroutine Flow Charts of MC Test Routine (Cont.)
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TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				MD GENERATION SUBROUTINE
41244	23	31000	31000	Clear Q and A.
41245	11	31000	54000	Generate W.P. in MD addresses 50000 through 51777.
41246	13	31000	54001	
41247	75	30176	41251	
41250	13	54000	54002	
41251	75	31600	41253	
41252	13	54000	54200	
41253	11	40000	40031	Set W.P. generation in MD indication.
41254	45	00000	00000	Jump back to test.
41255	11	40443	56000	Generate C.T.W.P. in MD addresses 56000 through 57177.
41256	13	40443	56001	
41257	75	30176	41261	
41260	13	56000	56002	
41261	75	31600	41263	
41262	13	56000	56200	
41263	11	40000	40032	Set C.T.W.P. generation in MD indication.
41264	45	00000	00000	Jump back to test.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41265	75	32000	41267	Transfer W.P. to MC.
41266	11	54000	00000	
41267	75	32000	41271	
41270	11	54000	02000	
41271	75	32000	41273	
41272	11	54000	04000	
41273	75	32000	41275	
41274	11	54000	06000	
41275	45	00000	40224	Jump back to test.
41276	75	32000	41300	Transfer K.W.P. to MC.
41277	13	54000	00000	
41300	75	32000	41302	
41301	13	54000	02000	
41302	75	32000	41304	
41303	13	54000	04000	
41304	75	32000	41306	
41305	13	54000	06000	
41306	45	00000	40274	Jump back to test.

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TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41307	75	32000	41311	Transmit C.T.W.P. to MD.
41310	11	56000	00000	
41311	75	32000	41313	
41312	11	56000	02000	
41313	75	32000	41315	
41314	11	56000	04000	
41315	75	32000	41317	
41316	11	56000	06000	
41317	45	00000	40400	Jump back to Test G.
41320	75	32000	41322	Transmit K.C.T.W.P. to MC.
41321	13	56000	00000	
41322	75	32000	41324	
41323	13	56000	02000	
41324	75	32000	41326	
41325	13	56000	04000	
41326	75	32000	41330	
41327	13	56000	06000	
41330	45	00000	40471	Jump back to Test H.

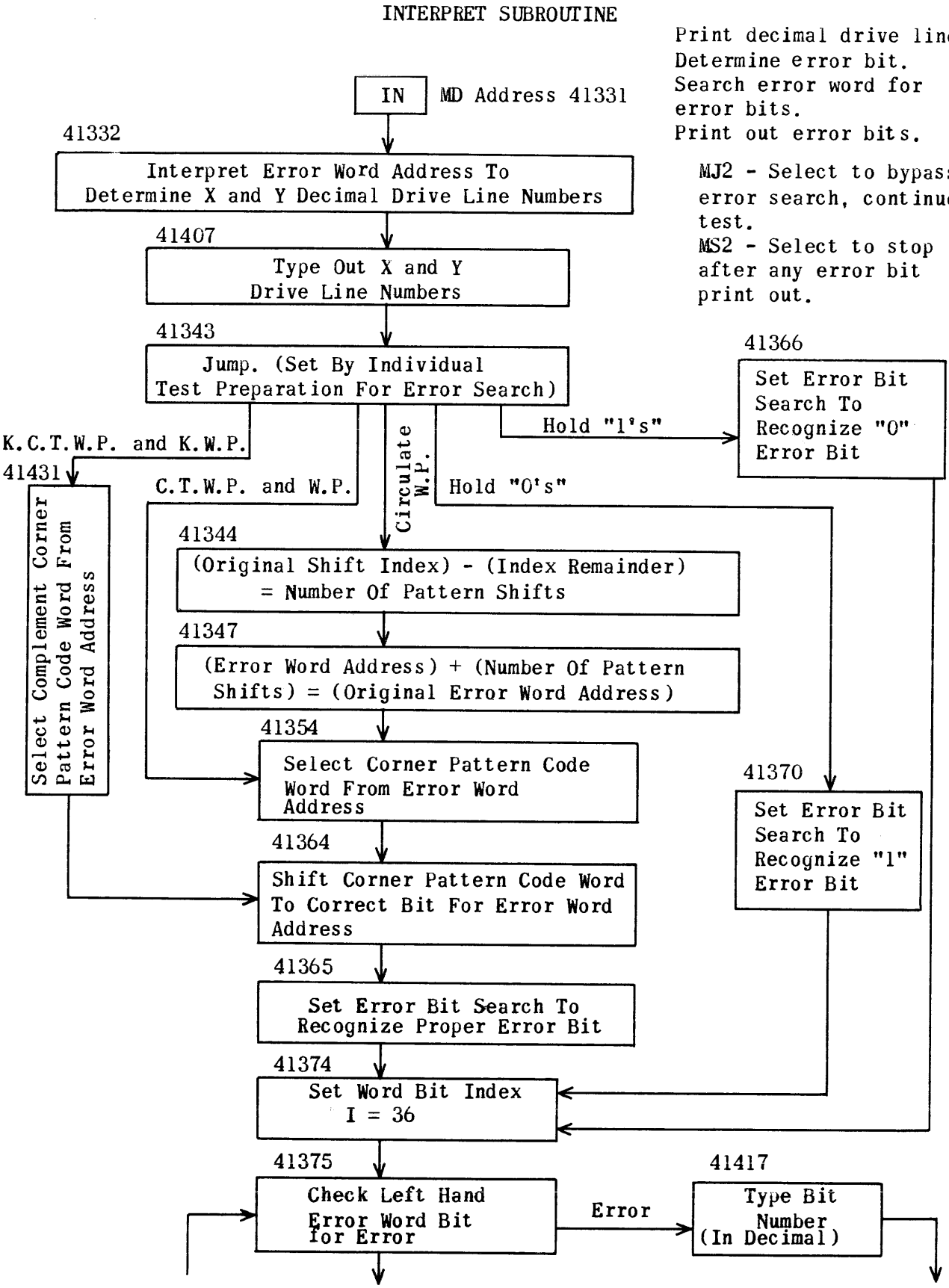

Figure 18. Interpret Subroutine Flow Chart of MC Test Routine
PX 142

INTERPRET SUBROUTINE (Cont.)

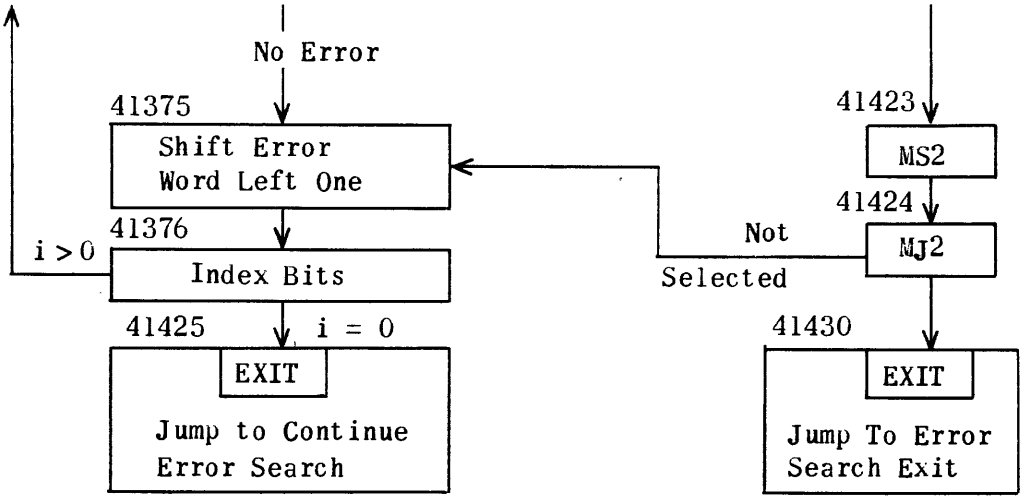

Figure 18. Interpret Subroutine Flow Chart of MC Test Routine (Cont.)
PX 142

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				INTERPRET SUBROUTINE
41331	11	41435	41452	Store error address.
41332	55	41452	00036	Transmit error address to Q, and shift Q left 30 places.
41333	51	41471	32000	Transmit y-drive line to A.
41334	61	00000	41443	Type "y".
41335	37	41425	41407	Jump to type y-drive line decimal number.
41336	61	00000	41440	Type "space".
41337	11	41435	31000	Transmit error address to Q.
41340	51	41471	32000	Transmit X drive line to A.
41341	61	00000	41442	Type "x".
41342	37	41425	41407	Jump to type x-drive line decimal number.
41343	45	00000	00000	Jump to interpret error bit.
41344	11	41435	41452	Store error word address.
41345	11	41450	41447	Set up original circulation count.
41346	23	41447	41437	Obtain worst pattern circulation numbers.
41347	21	41452	41447	Obtain error word original address and store.
41350	45	00000	41355	Jump to next instruction.
41351	00	00000	00000	Unused addresses.
41352	00	00000	00000	
41353	00	00000	00000	
41354	11	41435	41452	Store error word address.
41355	55	41452	00011	Shift error word address left 9 places.
41356	31	41445	00000	Transmit basic error bit code word transfer instruction to A.

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TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41357	52	41444	41363	Form error bit code word transfer instruction.
41360	31	41446	00000	Transmit basic shift instruction to A.
41361	55	31000	00033	Shift error word address back to original location.
41362	52	41444	41364	Form error bit code word shift instruction.
41363	00	00000	00000	Code word ⟶ Q.
41364	00	00000	00000	Shift code word to determine error bit.
41365	44	41366	41370	Detect error bit.
41366	11	41451	41372	Set bit search for "0" error bit.
41367	45	00000	41371	Jump to type space.
41370	11	41453	41372	Set bit search for "1" error bit.
41371	61	00000	41373	Type space.
41372	00	00000	00000	Transmit error word to Q.
41373	11	41454	32004	Set bit index in A.
41374	16	41403	41425	Set decimal type out exit jump.
41375	44	41404	41376	Error bit search.
41376	41	32000	41400	
41377	45	00000	41427	
41400	44	41404	41401	
41401	41	32000	41403	
41402	45	00000	41427	
41403	44	41404	41426	
41404	61	00000	41440	Type space.
41405	11	31000	41436	Store error word.
41406	11	32000	41473	Store working bit index.

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TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41407	73	41455	31000	Divide (A) by 12 octal to convert to decimal equivalent.
41410	35	41412	41422	Add the least significant digit of the error bit to the basic type instruction.
41411	45	00000	41413	Jump to form most significant digit type instruction.
41412	61	00000	41456	Basic type instruction operand.
41413	11	31000	32000	Transmit most significant digit of error bit to A.
41414	35	41416	41417	Add the most significant digit of the error bit to the basic type instruction.
41415	45	00000	41417	Jump to MD address 41417.
41416	61	00000	41456	Basic type instruction operand.
41417	00	00000	00000	Type most significant error bit digit.
41420	11	41436	31000	Transmit current error word to Q.
41421	11	41473	32000	Transmit bit index to A.
41422	00	00000	00000	Type least significant decimal digit.
41423	56	20000	41424	Stop if MS2 is selected.
41424	45	20000	41151	Omit further error information typeout if MJ2 is selected.
41425	45	00000	00000	Jump out of decimal type out sequence.
41426	41	32000	41375	Index error word bits.
41427	61	00000	41441	Type carriage return.
41430	45	00000	00000	Jump to leave Interpret Subroutine.
41431	11	41435	41452	Transmit error word address to MD address 41452.
41432	55	41452	00011	Transmit error word to Q and shift Q left 9 places.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
41433	31	41472	00000	Transmit MD address 41472 to A.
41434	45	00000	41357	Jump to MD address 41357.
41435	00	00000	00000	Storage location for current error word address.
41436	00	00000	00000	Storage location for current error word.
41437	00	00000	00000	Storage location for circulate W.P. index remainder.
41440	31	46314	00004	Error bit code word / Type code for space.
41441	31	46314	00045	Error bit code word / Type code for carriage return.
41442	46	31463	00027	Error bit code word / Type code for "x".
41443	46	31463	00025	Error bit code word / Type code for "y".
41444	00	00003	00003	Q mask operand.
41445	11	41440	31000	Basic error bit code word transfer instruction operand.
41446	55	31000	00000	Basic error bit code word shift instruction operand.
41447	00	00000	00000	Temporary W.P. shift count storage location.
41450	00	00000	00400	W.P. shift count operand.
41451	13	41436	31000	Set bit search for "0" error bit instruction operand.
41452	00	00000	00000	Storage location for error word address.
41453	11	41436	31000	Set bit search for "1" error bit instruction operand.
41454	00	00000	00043	Bit index.
41455	00	00000	00012	Decimal conversion operand.

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TABLE 3. MC TEST ROUTINE (Cont.)

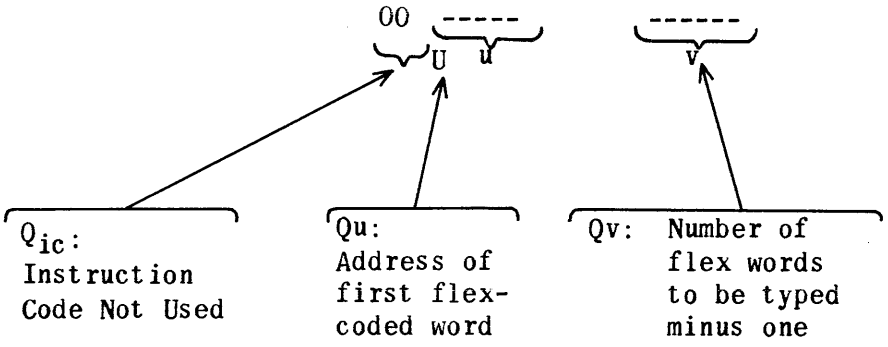
ADDRESS	OP-CODE	u	v	FUNCTION
41456	00	00000	00037	0
41457	00	00000	00052	1
41460	00	00000	00074	2
41461	00	00000	00070	3
41462	00	00000	00064	4
41463	00	00000	00062	5 Decimal digit type codes.
41464	00	00000	00066	6
41465	00	00000	00072	7
41466	00	00000	00060	8
41467	00	00000	00033	9
41470	00	00000	41370	Alter Interpret Subroutine operand.
41471	00	00000	00077	Drive line mask operand.
41472	13	41440	31000	Basic complement error bit code word transfer instruction operand.
41473	00	00000	00000	Storage location for working bit index.
41474	00	00000	00000	Unused address.
41475	00	00000	41366	Alter Interpret Subroutine operand.
41476	00	00000	41354	Alter Interpret Subroutine operand.
41477	00	00000	41344	Alter Interpret Subroutine operand.
41500	00	00000	41431	Alter Interpret Subroutine operand.

TABLE 3. MC TEST ROUTINE (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
				TYPE TEXT SUBROUTINE
41501	15	31000	41504	Code word address to u portion of MD address 41504
41502	16	31000	41513	Code word index to v portion of MD address 41513.
41503	11	41515	31045	Index mask to Q.
41504	31	00000	00052	Transmit type code word to A and shift A left 42 places.
41505	61	00000	32000	Type out the character in the two least significant bits of A.
41506	34	32000	00006	Clear A_R; shift A left 6 places.
41507	44	41510	41505	If Q_{35} is 1 take (u) as the next instruction. If Q_{35} is 0 take (v) as the next instruction.
41510	21	41504	41514	Add 00001 to u-portion of MD address 41504
41511	41	41513	41504	Check code word index; reduce index by 1.
41512	45	00000	00000	Jump to exit type text subroutine.
41513	00	00000	00000	Storage address for type code word index.
41514	00	00001	00000	Advance address operand.
41515	01	01010	10101	Q shift mask.

TYPE TEXT SUBROUTINE

Print packed type-code words as determined by type parameter word stored in Q. Type parameter word of the form:



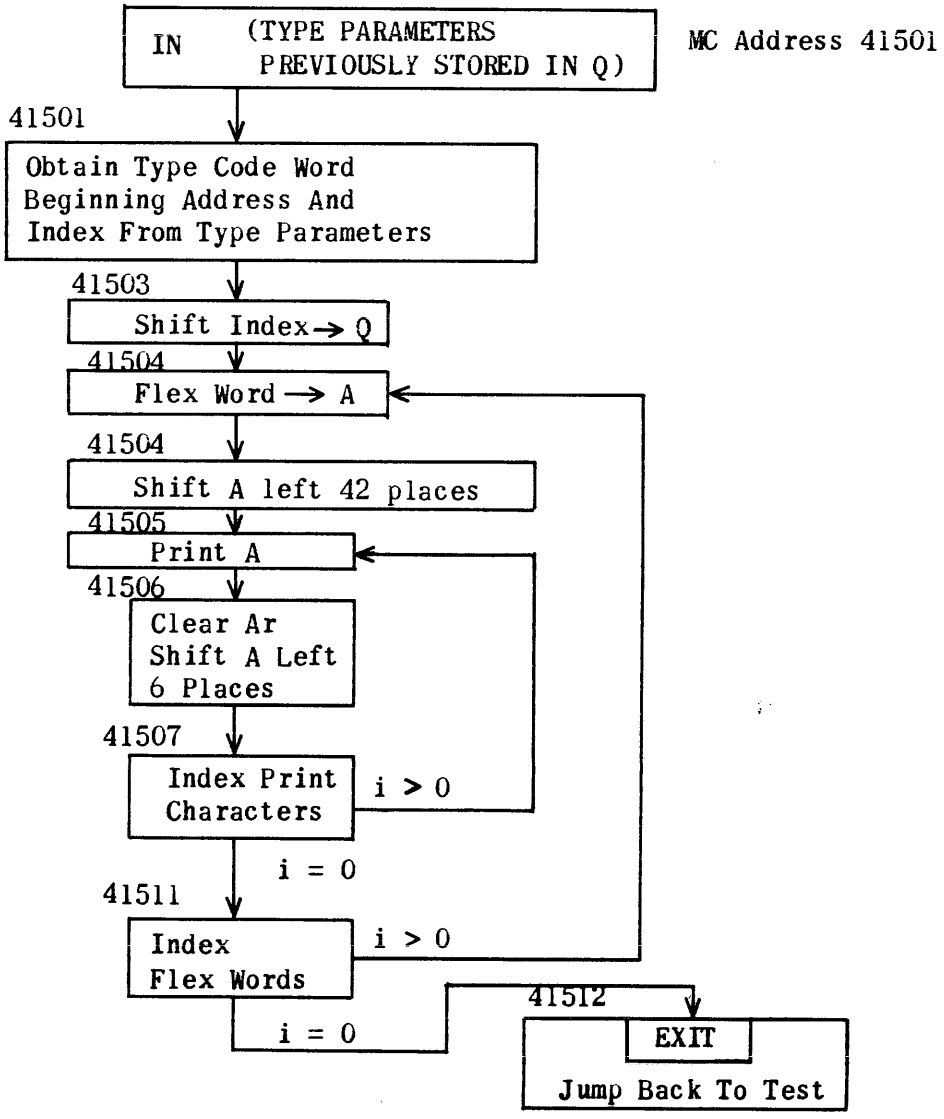


Figure 19. Type Text Subroutine Flow Chart of MC Test Routine PX 142

PUNCHED TAPE TEST

1. GENERAL

The punched tape test routine checks the operation of the High-Speed Punch and the Ferranti Tape Reader.

The test is performed in two parts. First, the test generates a punched tape consisting of a leader, a series of random numbers, and a trailer. Second, the generated tape is inserted in the Ferranti Reader and checked against the original generated pattern. If an error occurs, a zero stop is produced. If no errors occur, the typewriter prints "OK".

2. PROCEDURE

The punched tape test, contained on the master test tape, is stored on the drum in addresses 44000 through 44172. To run the test, proceed as follows:

1. PART ONE.

   Step 1. Insert paper in the typewriter, and set the typewriter switch to ON.

   Step 2. Set the toggle switch on the high-speed punch to the "up" position.

   Step 3. Make the following settings and selections:

   OPERATION MODE GROUP - - - - TEST

   START SELECTION - - - - - - MD START

   Set PAK TO 44000

   OPERATING GROUP - - - - - - START

   Step 4. After the generated tape issues from the high-speed punch, turn off the punch by setting the toggle switch to the "down" position.

2. PART TWO.

   Step 1. Enter the generated tape in the Ferranti Reader.

   Step 2. Press the OPERATING GROUP "START" button.

3. THEORY OF PART ONE

Instructions 44000 and 40001, repeated, transmit the test routine to MC, then produce a jump to the test routine at 00066. Instructions 00066 through

00072 cause the typewriter to print "PT TEST", then execute a jump to 00032. Instruction 00032 transmits the line index to Q, 00033 is an MS1 to change the line index value, 00034 transmits the line index to A, and 00035 reduces the line index by one. If the index is then zero, an error has occurred and an error stop is produced by 00036. If the index is not zero, a jump to 00037 follows. Instruction 00037 stores the line index in 00055, and instruction 00040 stores the same line index in 00053.

Instructions 00041 and 00042, repeated, punch a tape leader, 00043 punches a seventh level hole, and instructions 00044 and 00045 punch 32 lines of zeros. Instruction 00046 initiates an indexed cycle in which a series of random numbers are generated and punched on the test tape.

In this cycle instruction 00046 modifies the program, then produces a jump to the random number generator at 00003. Instructions 00003 through 00005 generate a number in A and store the number at 00002. Instruction 00006 produces a jump to 00047 which then modifies the program and produces a jump to the random number punch routine at 00007. Instructions 00007 through 00012 punch the random number, and 00013 produces a jump to the index jump at 00050. Instruction 00050 subtracts one from the line index. If the index does not equal zero, a jump to 00046 follows, and the cycle is repeated.

At the end of the cycle, 00050 finds the index equal to zero, and a jump is produced to 00051. Instructions 00051 and 00052 punch the trailer, and then execute a jump to a zero stop at 00054.

4. THEORY OF PART TWO

After the tape has been inserted into the Ferranti Reader, the reader set to ON and the START pressed, the program resumes at 00100. Instructions 00100 and 00101 clear IOA, 00102 sets the line index for reading, 00103 starts the reader, and 00104 reads one line of tape to A. Instruction 00105 checks the content of A. If A is zero, a jump to 00104 is made, and the reading continues until a value other than zero appears in A. When such occurs, instruction 00106 is then executed, and the seventh level value 00100 is subtracted from A. If A is not zero, an error has occurred, and a zero stop is produced at 00107. If A is zero a jump to 00110 follows, the leader index is set up, and one line of the leader is read to A. Instruction 00112 reduces the index value by one, then produces a jump to continue the indexed cycle at 00111 if K is not zero, or, produces a jump to 00113 if K is equal to zero.

Instruction 00113 stops the Ferranti Reader, 00114 reads IOA to A, 00115 transmits the random number from storage to Q, and 00116 clears the random number storage. Instruction 00117 introduces an indexed cycle in which the mode of operation alternately stops or free runs the Ferranti during the reading and checking of the random numbers contained on the tape. Instruction 00117 sets up the mode index, and the next instruction selects the mode of operation in accordance with the value of A_{71}. If $A_{71} = 0$, a jump to the step mode at 00121 is produced, or, if $A_{71} = 1$, a jump is produced to the free run mode at 00123. In either case, the process of checking is essentially the same.

The Ferranti reads a single line of tape to IOA. The random number generator then generates the initial line of the random number in A. The lower seven bits of A are masked and the next instructions read, IOA to Q and subtract Q from A. Thus as the number generator reproduces one line of the original random number, the reader reads a line of the original from tape. If they are equal, A will equal zero. If A does not equal zero, an error has occurred, and a zero stop is produced. If A is equal to zero, the number is correct, the line index is then reduced by one, the mode index is reduced by one, and a return jump is made to check the next line of the random number. When the line index equals zero, a jump is produced to the print routine and "OK" is printed.

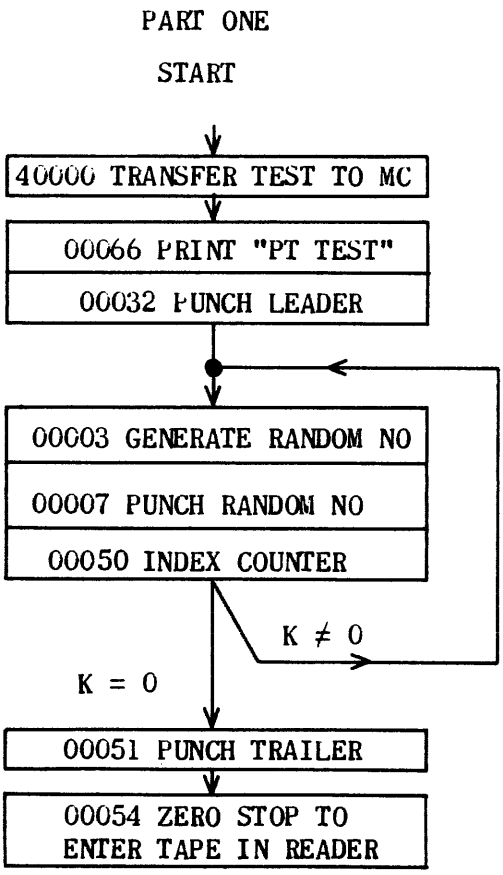


Figure 1. Punched Tape Test
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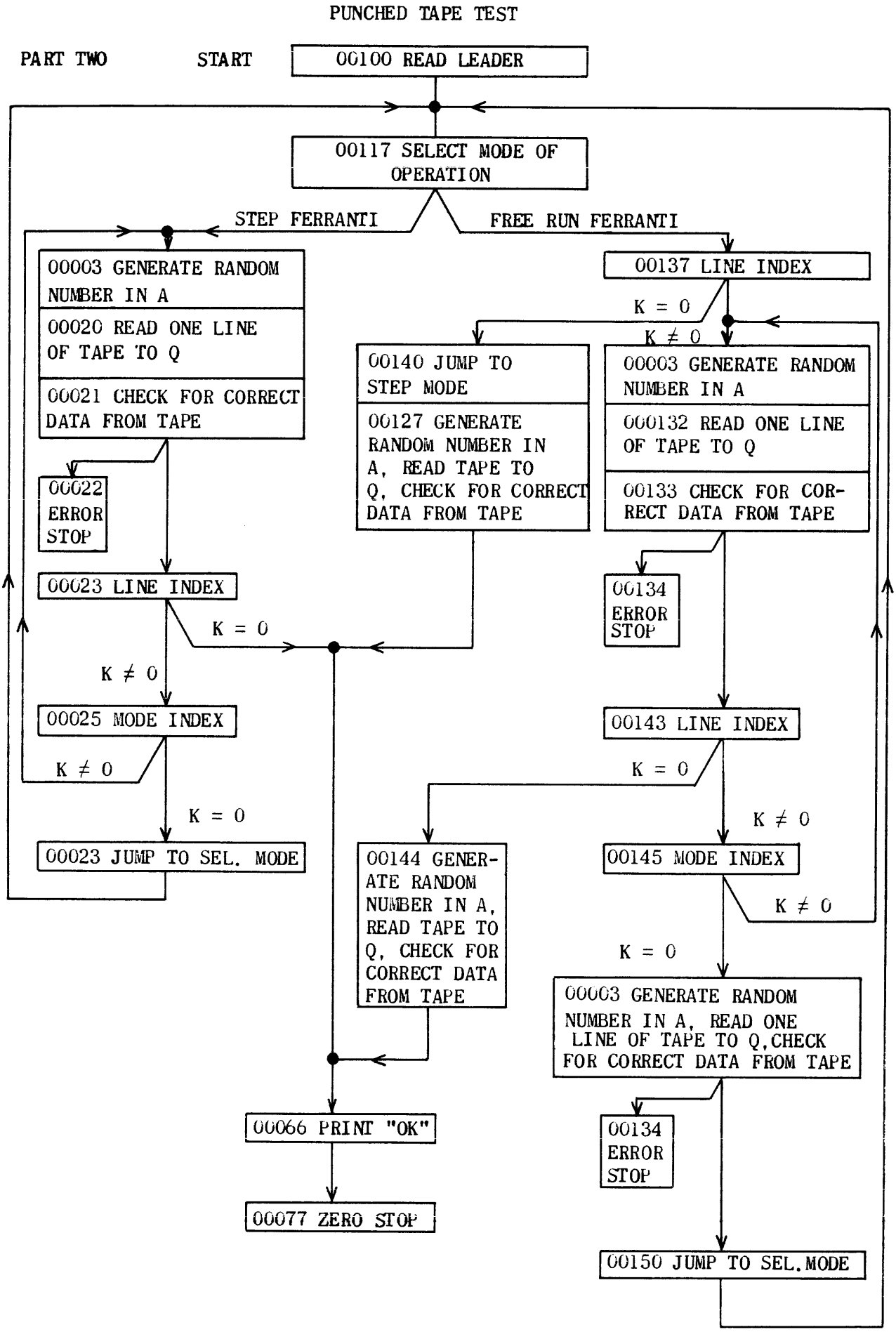

Figure 1. Punched Tape Test (Cont.)
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TABLE 1. PUNCHED TAPE TEST

PROGRAM: Punched Tape Test

DESCRIPTION: Punches random numbers on paper tape. The tape is then read back and compared to the original numbers. Shows failing number in Q and correct number in A after a final stop.

ADDRESS	OP-CODE	u	v	FUNCTION
44000	75	30170	00066	Block transfer to cores.
44001	11	44002	00000	
44002 thru 44172				See 00000 thru 00170.
00000	45	00000	00043	Jump to start.
00001	47	13501	60140	Constant number.
00002	00	00000	00000	Random number.
00003	71	00002	00001	Random number generator.
00004	32	00001	00105	
00005	11	32000	00002	
00006	45	00000	00000	
00007	11	32000	31000	Random number punch routine.
00010	54	32000	00025	
00011	15	32000	00012	
00012	63	00000	31000	
00013	45	00000	00000	
00014	17	00000	00164	Step Ferranti.
00015	37	00006	00003	Jump to generate random number.
00016	11	00062	31000	Mask to Q.
00017	51	32000	32000	Mask Lower 7 bits to A.

TABLE 1. PUNCHED TAPE TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00020	76	00000	31000	Compare routine read 1 line tape to Q.
00021	43	31000	00023	Check for correct data from tape.
00022	56	00022	00100	error stop.
00023	41	00056	00025	Count Line index down 1.
00024	45	00000	00066	jump to print "OK".
00025	41	00061	00014	Count down mode index 1.
00026	45	00000	00000	Jump to next selection.
00027	45	47150	40104	Packed Flex codes.
00030	01	20240	10404	
00031	47	03360	45704	
00032	11	00162	31000	Line index to Q.
00033	56	10000	00034	MS-1 to change line index.
00034	11	31000	32000	Line index to A.
00035	41	32000	00037	Reduce index by 1.
00036	56	00036	00032	error stop.
00037	11	32000	00055	Store index.
00040	11	32000	00053	
00041	75	00140	00043	Punch Leader.
00042	63	00000	00034	
00043	63	10000	00034	Punch 7th Level.
00044	75	00040	00046	Punch 32 lines of zeroes.
00045	63	00000	00034	
00046	37	00006	00003	Jump to generate number.
00047	37	00013	00007	Jump to punch generated number.

TABLE 1. PUNCHED TAPE TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00050	41	00053	00046	Count line index down 1.
00051	75	00100	00054	Punch trailer.
00052	63	00000	00034	
00053	00	00000	00000	Line index (punching).
00054	56	00000	00100	
00055	00	00000	00000	Line index storage, K.
00056	00	00000	00000	Line index (reading).
00057	00	00000	00036	Leader index (reading).
00060	00	00000	00000	
00061	00	00000	00000	Mode index k.
00062	00	00000	00177	Mask.
00063	00	00000	00017	Program constants.
00064	00	00000	00010	
00065	00	00000	00100	
00066	11	00157	31000	Print mask to Q.
00067	31	00027	00052	1st flex code to A_0-5.
00070	61	00000	32000	Print flex code.
00071	54	32000	00006	Shift next flex code to A_{0-5}.
00072	44	00070	00073	Check for finished packed flex word.
00073	15	00160	00067	Change packed word setup inst.
00074	37	00072	00067	Modify jumpout at end packed flex word.
00075	15	00161	00067	Changed packed word setup inst.
00076	37	00072	00032	Modify jumpout at end packed flex word.
00077	56	00000	00100	Stop, go to read routine.

TABLE 1. PUNCHED TAPE TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00100	17	00000	00164	Clear IOA.
00101	76	00000	01770	
00102	11	00055	00056	Set line index (read).
00103	17	00000	00165	Start Ferranti.
00104	76	00000	32000	Read 1 line data to A.
00105	47	00106	00104	Check for information.
00106	43	00065	00110	Check for 7th level.
00107	56	00107	00100	Error stop.
00110	11	00057	00060	Set Leader index (read).
00111	76	00000	32000	Read 1 line leader to A.
00112	41	00060	00111	Count leader 1 index (read) down 1.
00113	17	00000	00166	Stop Ferranti .
00114	76	00000	32000	Read last line leader to A.
00115	11	00002	31000	Random number to Q.
00116	23	00002	00002	Clear random number storage.
00117	51	00063	00061	Set up mode index.
00120	42	00064	00123	Select mode of operation.
00121	37	00026	00014	Jump to read step mode.
00122	45	00000	00124	Jump to next selection.
00123	37	00150	00137	Jump to read free run mode.
00124	11	00002	31000	Random number to Q.
00125	45	00000	00117	Jump to select mode of operation.
00126	00	00000	00000	
00127	37	00006	00003	Jump to generate random number.

TABLE 1. PUNCHED TAPE TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00130	11	00062	31000	Mask to Q.
00131	51	32000	32000	Mask lower 7 bits to A.
00132	76	00000	31000	Read 1 line of tape to Q.
00133	43	31000	00136	Check for correct data from tape.
00134	17	00000	00166	Stop Ferranti.
00135	56	00135	00100	Error stop.
00136	45	00000	00000	Jump back to free run program.
00137	41	00056	00141	Count down line index (reading)
00140	45	00000	00154	Jump to step Ferranti.
00141	17	00000	00165	Start Ferranti.
00142	37	00136	00127	Jump to read and check one line.
00143	41	00056	00145	Count down line index.
00144	45	00000	00151	Jump to stop Ferranti .
00145	41	00061	00142	Count down mode index.
00146	17	00000	00166	Stop Ferranti.
00147	37	00136	00127	Jump to read and check one line.
00150	45	00000	00000	Jump to next selection.
00151	17	00000	00166	Stop Ferranti.
00152	37	00136	00127	Jump to read and check one line.
00153	45	00000	00066	Jump to print "OK".
00154	17	00000	00164	Step Ferranti.
00155	37	00136	00127	Jump to read and check one line .
00156	45	00000	00066	Jump to type "OK" .
00157	76	76767	67676	Printing mask.

TABLE 1. PUNCHED TAPE TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
00160	00	00030	00000	Print constants.
00161	00	00031	00000	
00162	00	00000	05000	Line index-K.
00163	26	26262	62626	
00164	10	00003	00000	Code for step Ferranti.
00165	10	00002	00000	Code for start Ferranti.
00166	10	00001	00000	Code for stop Ferranti.

LONG COMMAND TEST

1. GENERAL

The Long Command Test Program consists of a series of 27 tests, parts A through Z and part 22. These tests check the performance of all computer instructions except those involving external equipment.

This is accomplished generally by the generation and manipulation of simple arithmetic quantities, followed by the checking of the results. As the program progresses, the tests increase in complexity. Each test introduces a new instruction, and the satisfactory completion of a test signifies that the instructions used up to that point are functioning properly. When a failure occurs, the letter identifying the failing test is printed by the typewriter.

2. PROCEDURE

Normally, the command test program will have been loaded on the drum in preparation for the maintenance run. If, however, the program is not present, the command test tape may be loaded on the drum beginning at address 46000.

To run the test, perform the following operations:

Step 1. Insert paper in the typewriter, set the typewriter power switch to the ON position, and select ON LINE in the typewriter controls.

Step 2. In the Test Switch Group on the Supervisory Control Panel, set the TEST-NORMAL switch to TEST; set all of the Test Switch Group AMPLIFIER MARGINAL CHECK switches to the "up" position if the test is to be executed on high margin, or, if the test is to be executed at low margin. to the LO position.

Step 3. Make the following sequence of selections:

Set PAK to 46000

Optional selections described below

Operating Group - - - START

Optional STOP selections may be made at any time. The JUMP selection may be made or dropped only when the computer is stopped. Select these as follows:

1) SELECTIVE STOPS GROUP --- SELECT STOP 1 at any time to stop at the end of each successful test section (Test A, Test B, etc.)

2) SELECTIVE JUMPS GROUP --- SELECT JUMP 1 after a stop to cause the last-executed test section to be repeated.

3) SELECTIVE STOPS GROUP --- SELECT STOP 2 at any time to stop at the successful completion of the entire test if MJ2 previously has been selected.

4) SELECTIVE JUMPS GROUP --- SELECT JUMP 2, when stopped, to cause the entire test to be repeated at the end of a successful run.

5) SELECTIVE STOPS GROUP --- SELECT STOP 3 at any time to produce a stop after a failure.

3. THEORY OF THE TEST

After a START selection has been made, instruction 46000 stores a Jump instruction at F_1. Next, 46001 executes a jump to 46002. Repeat instruction 46002, and repeat Transmit Positive 46003 and transmit the Long Command Test Routine to consecutive rapid-access storage addresses starting with address 01000. Next, a jump is executed to 01000.

Instructions 01000 through 01016 operate the typewriter to print "COMMAND TEST". Instruction 01017 clears A and Q, and the program continues with 01020, the start of Test A.

In each test, a Print (61-v) instruction and a Manually Selective Jump (45jv) instruction with j = 0 are executed if an error is detected. The Print instruction prints the identifying test letter, and the Manually Selective Jump instruction produces a jump to a routine which types "FAILED" and then produces a stop if the SELECT STOP 3 has been pressed. Pressing the START button after this stop occurs causes the entire test program to be restarted at 01000.

The last two instructions in each test are a Manually Selective Stop (56jv) instruction with j = 1, followed by a Manually Selective Jump instruction with j = 1. If no errors occur during a test, execution of the 56jv produces a stop if the SELECT STOP 1 button has been pressed; execution of the 45jv instruction produces a jump to repeat the current test if the SELECT JUMP 1 button has been pressed.

1) TEST A. - At the beginning of Test A, the contents of Q and A are zero. Instruction 01020 transmits 36 zeros from Q to A, then instruction 01021 checks the contents of A. If an error is detected, "A FAILED" is printed. If no errors are detected, the test is repeated if SELECT JUMP 1 has been pressed.

2) TEST B. - At the beginning of Test B, the contents of Q and A are zero. Instruction 01026 transmits the complement of (A) to Q to set (Q) to 36 ones. Next, the 36 ones from Q are transmitted to A. The resulting borrow in A sets A to all zeros if no errors occur. Instruction 01030 checks the contents of A, and the test is terminated in the same manner as Test A.

3) TEST C. - At the beginning of Test C, the Q register contains 36 ones, and A contains all zeros.

If no error occurred in the Index Jump execution, 01036 transmits the complement of (A) to Q, which leaves Q set to +1. Next, 01037 transmits a

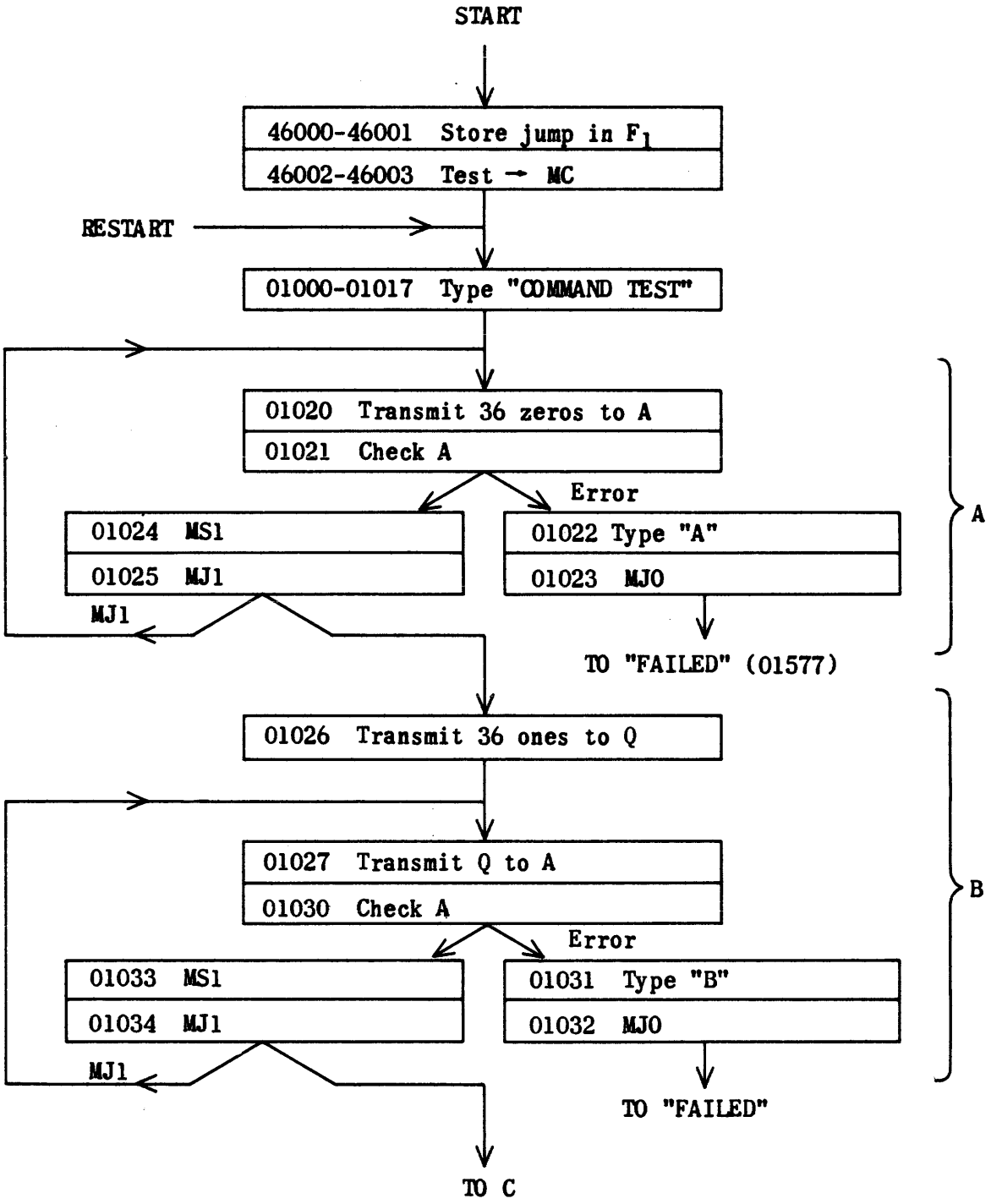

Figure 1. Parts A and B of Command Test
PX 144

Manually Selective Jump instruction into address 01047, then Return Jump instruction, 01040, inserts the value of the current address plus one (01041) into the v-address portion of 01047 and executes a jump to 01046.

If the jump portion of the Return Jump instruction is executed properly, 01046 is taken. This instruction complements (A) so that it is +1. Instruction 01047 is executed next. If the v-address portion of 01047 is equal to 01041, indicating that the insert portion of the Return Jump was executed properly, 01047 produces a jump to 01041.

The execution of 01041 checks (A) against (Q). If no errors have occurred up to this point, (Q) and (A) are both +1, and a jump to 01043 occurs. Index Jump instruction 01043 subtracts one from (A) and executes a jump to 01050. If no errors occurred, the test is terminated in the same manner as each of the preceding tests by execution of 01050.

During Test C, a jump to the error print-out at 01044 is executed if one of the following types of errors occurs: (1) if Index Jump 01035 fails to subtract one from (A) properly, leaving (A) zero, (2) if Return Jump 01040 fails to execute the jump so that 01041 and 01042 are executed, (3) if Return Jump 01040 fails to alter the v-address portion of 01047, (4) if the normal execution of 01041 fails to find (A) +1, or (5) if the execution of Index Jump 01043 fails to produce a jump to 01050.

4) TEST D. - At the beginning of Test D, (A) is zero and (Q) is +1. A repeated cycle consisting of 01052 and 01053 alternately adds (Q) to (A), inspects (Q), and shifts (Q) left so that after 36 cycles a number consisting of 36 ones has been added to (A). In (A), this sum becomes zero if no errors have occurred. Instruction 01054 checks (A), and the test is terminated in the usual manner.

5) TEST E. - At the beginning of Test E, (Q) is +1 and (A) is zero. Instruction 01061 complements (Q) to -1, which is 35 ones and one zero. A cycle consisting of 01062 and 01063, performed 36 times, alternately subtracts (Q) from (A) and shifts (Q) so that effectively a number consisting of 36 zeros is subtracted from (A). Instruction 01064 checks (A), which should be zero. Next, the test is terminated in the usual manner.

6) TEST F. - At the beginning of Test F, (Q) is 35 ones and one zero (-1), and (A) is all zeros. A repeated cycle consisting of 01071 and 01072 alternately adds (Q) to (A) and shifts (Q) left so that effectively a number consisting of 36 zeros is added to (A). Instruction 01073 checks (A), which should be zero. The test is terminated in the usual manner.

7) TEST G. - At the beginning of Test G, Q contains 35 ones and one zero (-1), and A contains all zeros. Instruction 01100 complements (Q) to form +1 in Q. A repeated cycle consisting of 01101 and 01102 alternately subtracts (Q) from (A) and shifts (Q) left so that a number consisting of 36 ones, the equivalent of zero, is effectively subtracted from (A). Next, 01103 checks (A), and the test is terminated as usual.

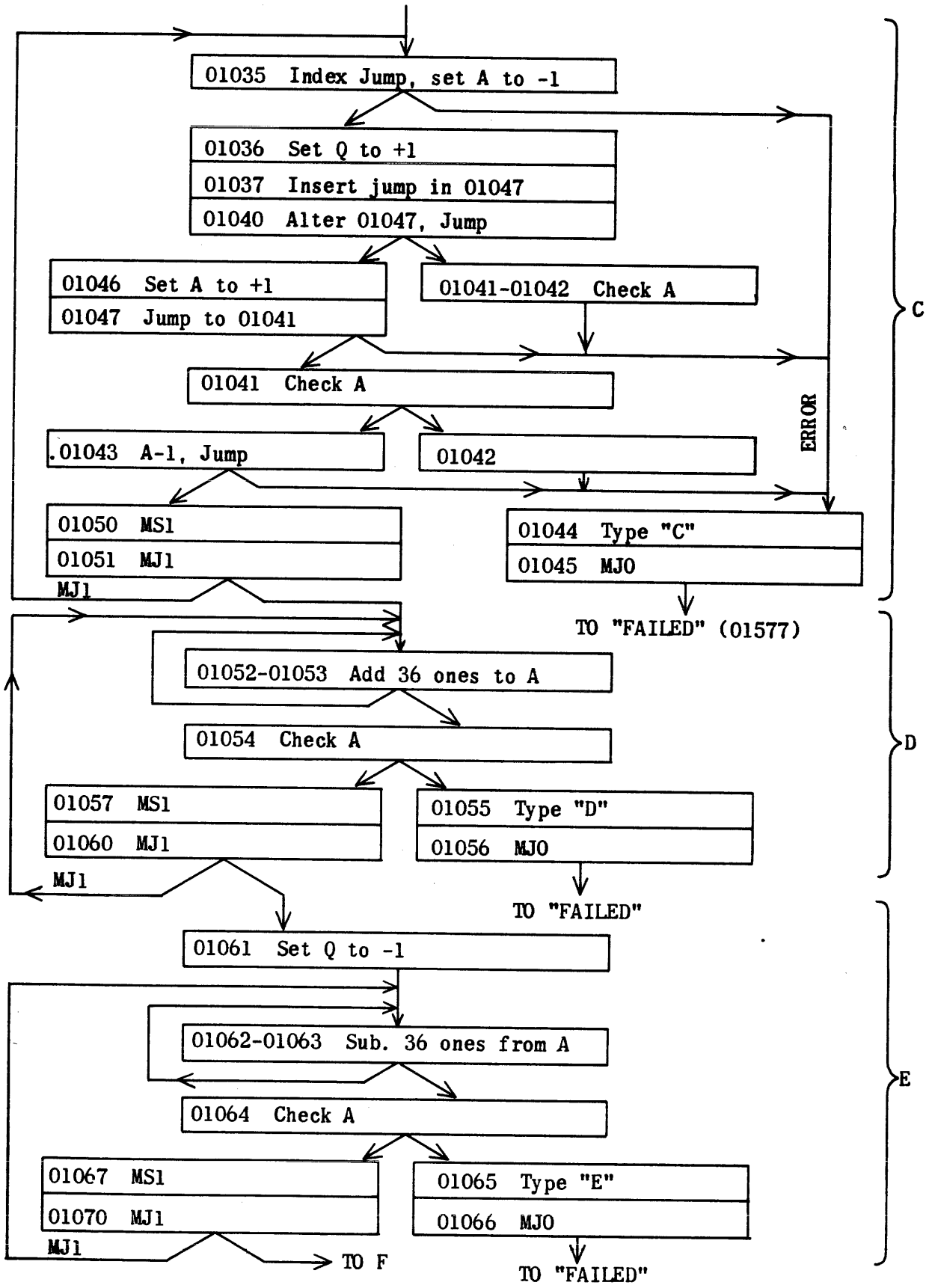

Figure 2. Parts C, D, and E of Command Test
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8) TEST H. - At the beginning of Test H, (Q) is +1 and (A) is zero. A repeated cycle consisting of 01110 and 01111 alternately adds (Q) to (A) and shifts (A) left one place until (A) is filled with 71 ones and one zero. Next, 01112 adds an additional one to (A), and the resulting borrow in (A) should set (A) to all zeros. Next, 01113 checks (A), and the test is terminated.

9) TEST I. - At the beginning of Test I, (Q) is +1 and (A) is zero. The repeated cycle consisting of 01120 and 01121 alternately subtracts (Q) from (A) and shifts (A) left once until 71 ones have been split-subtracted from (A). Effectively, a number consisting of 71 ones and one zero, equivalent to -1, is subtracted from (A). The resulting sum in (A) is +1. Next, 01134 subtracts (Q) from (A), which should restore (A) to all zeros. Next, 01123 checks (A), and the test is terminated as usual.

10) TEST J. - At the beginning of Test J, (Q) is +1 and (A) is zero. Instruction 01130 sets (Q) to all ones by transmitting the complement of (A_R) to Q. Next, 01131 inserts digits in both the left and right halves of A by split-adding 36 ones to (A) and shifting (A) left 18 places. Instruction 01132 clears A, enters 36 ones in A_R, and shifts these ones to A_L. Next, 01133 inserts 36 ones in A_R, and the resulting borrow in (A) sets (A) to all zeros. If an error has occurred so that A is not cleared during 01132, (A) is not zero. Instruction 01134 checks (A), and the test is terminated as usual.

11) TEST K. - At the beginning of Test K, Q contains 36 ones (-0), and A contains all zeros. Instruction 01141 inserts digits in both the left and right halves of A by adding 36 ones to (A_R) and shifting (A) left 18 places. Instruction 01142 clears A, adds the complement of (Q) to (A), and shifts (A) left 36 places. This fills A_R with ones and A_L with zeros. Next, 01143 subtracts the 36 ones from (A_R) so that (A) should be zero. Instruction 01144 checks (A), then the test is terminated.

12) TEST L. - At the beginning of Test L, (A) is zero. Instruction 01151 sets an index operand, 01172, to a starting index value equal to 4096. Next, an indexed cycle performed 4097 times checks the performance of A.

Each time the indexed cycle is performed, 01152 sets (Q) to the current index value n. Instructions 01153, 01154, and 01155 form 2n in (Q) and n in (A), then subtract (Q) from (A) to leave -n in (A). Next 01156, 01157, and 01160 form -2n in A and -n in Q, then subtract (Q) from (A) to leave -n in A. Next 01161, 01162, and 01163 form -n in A and -2n in Q, then subtract (Q) from (A) to leave +n in A. Next 01164, 01165, and 01166 form +2n in A and +n in Q, and subtract (Q) from (A) to leave +n in A. Instruction 01167 subtracts n from (A) to leave all zeros in A, if no errors occur. 01170 checks (A) and produces a jump to Index Jump 01175, which causes the indexed cycle to be repeated with a new index number. If an error occurs during any cycle, 01170 produces a jump to the error print-out. If no errors occur, the test is terminated as usual.

13) TEST M. - At the beginning of Test M, (A) is zero. Instruction 01200 sets (Q) to a starting "n" value of 4096. Next, an indexed cycle starting at 01201 is performed 4097 times. In the indexed cycle, three checks are performed to determine whether (A) is equal to (Q). If errors occur at these points, jumps are executed to 01215 which leads to the error print-out.

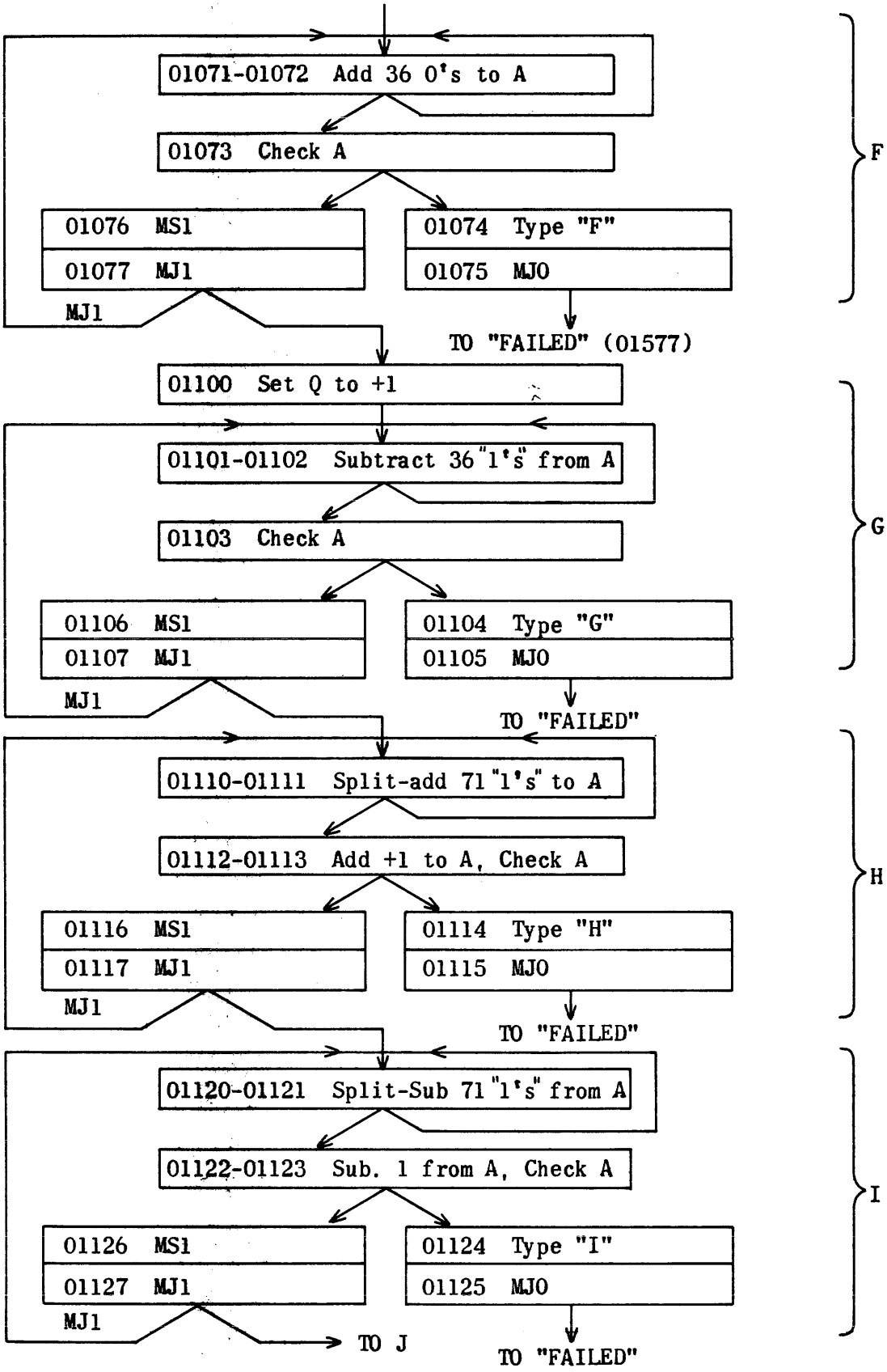

Figure 3. Parts F through I of Command Test
PX 144

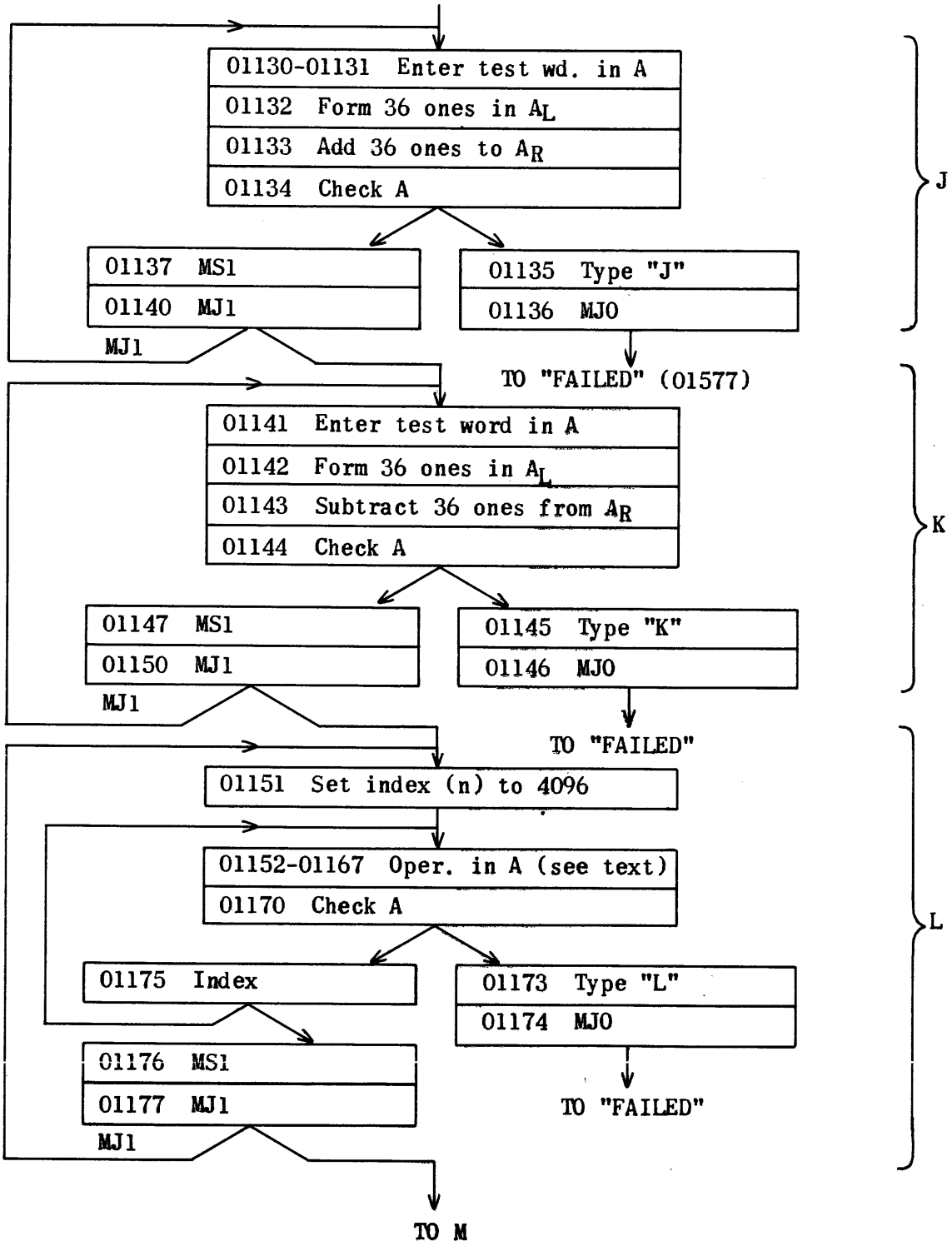

Figure 4. Parts J, K, and L of Command Test
PX 144

During each performance of the indexed cycle, 01201 transmits n from Q to A. Instruction 01202 performs the first check to determine if (Q) = (A). A jump to 01205 complements (A) to set (A) to -n. The second check, 01206, produces a jump to 01203 if (A) is different from (Q) (error). If no error has occurred, 01207 recomplements (A) to +n, and the third check is performed by 01210. If (A) is equal to (Q), a jump to 01213 is executed. Index Jump instruction 01213 merely reduces n (stored in Q) by one count. Index Jump 01214 subtracts one from n, stored in A. and jumps to 01201 if (A) is positive. As a result, the indexed cycle is performed 4097 times. The error and no-error terminations are similar to all the other tests.

14) TEST N. - At the start of Test N, (A) and (Q) are both -1. Instruction 01217 sets (Q) to +1 by transmitting the complement of (A) to (Q). Next, 01220 sets index 01225 to the value 4096.

An indexed cycle starting at 01221 is performed 4097 times. Instruction 01221 clears A. Next, 01222 and repeated instruction 01223 form the sum of the following series in A;

$$S = \sum_{i=0}^{i=11} 2^{6i}\, n$$

Next, a subcycle consisting of 01226, 01227, and 01230 is performed 36 times. During each subcycle, (Q) is added to (A), then (A) is added to (Q). The Q-Jump instruction 01230 controls the subcycle by producing a jump to 01226 if Q35 = 0. Because each execution of 01230 shifts (Q) left one place, each subcycle adds and subtracts a new value to (A). Because (Q) is initially +1, the subcycle is executed 36 times. Next, 01231 and repeated instruction 01232 subtract the sum of the series S from (A), which reduces (A) to zero. If an error occurs during one of the indexed cycles, 01233 produces a jump to 01234 so that "N FAILED" is printed and the test is terminated. If no errors occur, a jump to 01236 is executed. Index Jump instruction 01236 causes the test cycle to be repeated. After the 4096th execution of 01236, the test is terminated.

15) TEST O. - At the beginning of Test O, (A) is zero. Instruction 01241 transmits an initial index value n into Q. Next, an indexed cycle starting at 01242 is performed 4097 times.

During each performance of the indexed cycle, 01242 transmits n from Q to storage address 01253, 01243 transmits the complement of n, (-n), from Q to 01254, 01244 forms n-1 in 01253, 01245 forms 1-n in 01254, and 01246 forms n-1 in A. Next 01247 checks for errors by comparing the contents of 01253 with (A). If the two are not equal, 01250 and 01251 are executed to print "O FAILED". If no errors have occurred, 01247 executes a jump to 01256. Index jump 01256 reduces (Q) by one count, then if (Q) is positive a jump is made to the no-error termination.

16) TEST P. - Instruction 01261 clears (A) and (Q). During this test, four checks are made. If any of the checks determine that an error has occurred, a jump is made to 01265 so that "P FAILED" is eventually printed.

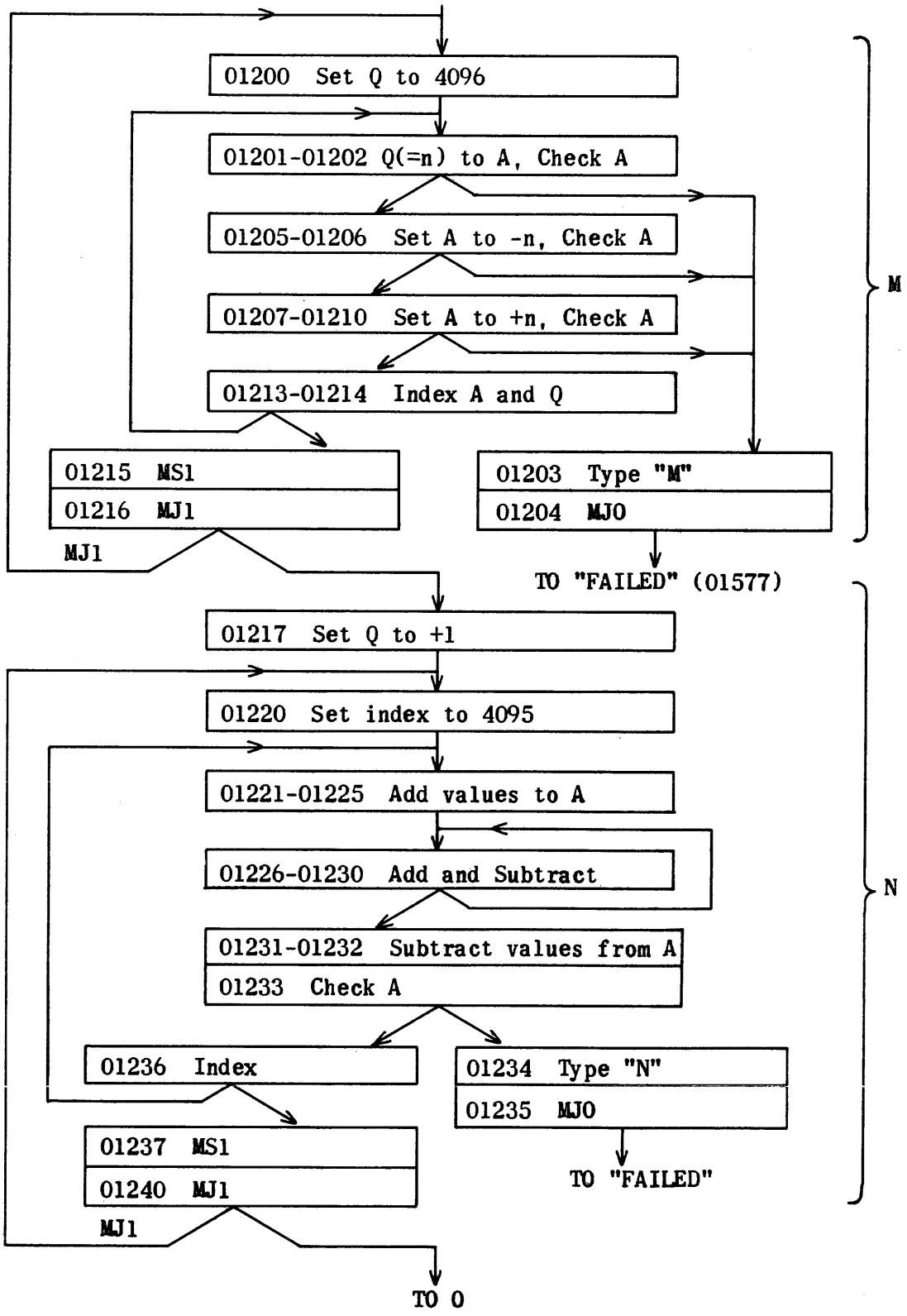

Figure 5. Parts M and N of Command Test
PX 144

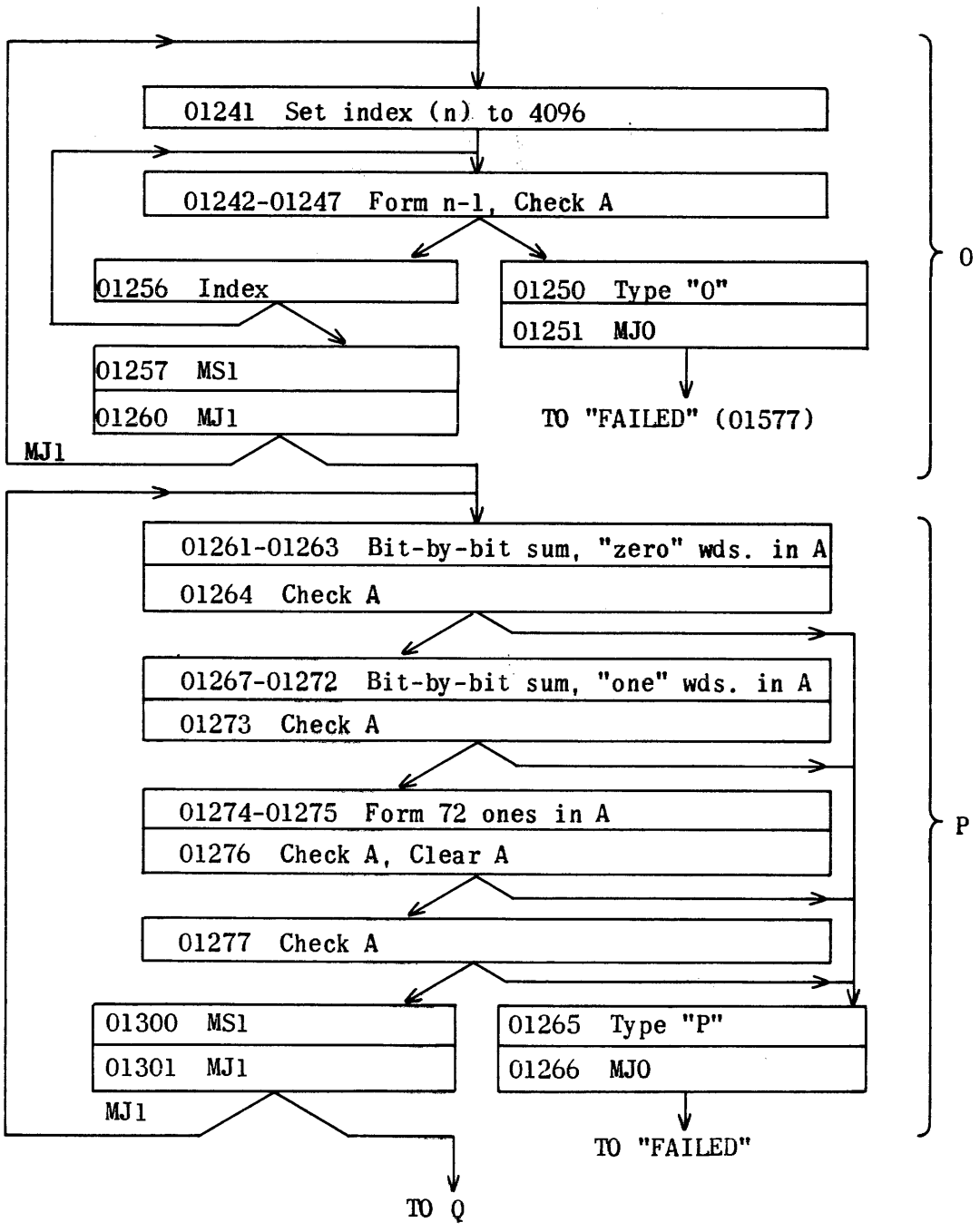

Figure 6. Parts O and P of Command Test
PX 144

Instruction 01262 forms the bit-by-bit sum of (Q) plus (Q) in A_R, which should be zero. Next, instruction 01263 adds (Q) to (A), and 01264 performs the first check. If no errors occur, (A) is zero and a jump to 01267 is executed.

Instruction 01267 complements (Q) to all ones, 01270 forms the bit-by-bit sum of (Q) plus (A) in A_R, and 01271 shifts (A) left 36 places. As a result, 36 ones are left in A_L and 36 zeros are left in A_R. Next, 01272 split-adds the 36 ones in Q to (A), and the resulting borrow in A clears (A) to all zeros. The second check is performed by 01273. If no errors occur, (A) is zero, and 01273 is followed by 01274.

Instruction 01274 enters the 36 ones from Q in A_R and shifts (A) left 36 so that A_L contains 36 ones. Next, 01275 forms the bit-by-bit sum of (Q) and (A_R) in A_R. As a result, A contains 72 ones. Instruction 01276 performs the third check. If an extraneous borrow was produced in (A) during 01275 so that (A) is zero, a jump to the error termination is made.

If no errors occur, the arithmetic functions performed during the Zero Jump instruction 01276 leaves (A) set to all zeros. Next, 01277 performs the fourth check. If no errors have occurred, (A) is zero, and the test terminates with 01300 and 01301.

17) TEST Q. - Instruction 01302 sets index 01312 to the value 33. Next, 01303 sets (Q) to a test value 2×8^{11}. An indexed cycle performed 34 times starts at 01304.

Two checks are executed during each performance of the indexed cycle. Instruction 01304 clears (A), and 01305 produces a jump to 01313 if (Q) is larger than (A). If an error occurs, no jump is produced by 01305, and instruction 01306 starts the printing of "Q FAILED". Instruction 01313 performs a second check by testing the contents of A. If (A) is not zero, a jump is made at this time to print "Q FAILED". If no errors occur during the test cycle, 01314 shifts (Q) left 35 places to alter the test value in Q, and then Index Jump 01327 causes the cycle to be repeated 33 times.

18) TEST R. - Instruction 01320 resets the index 01312 to the value 33, and 01321 resets (Q) to 2×8^{11}. An indexed cycle performed 34 times starts at 01322.

During each performance of this indexed cycle, two checks are executed. Instruction 01322 adds a test value to (A) and shifts (A) left 37 places. The first check is performed by 01323, which subtracts (Q) from (A) and jumps to print "R FAILED" if (A_{71}) is one. If no errors have occurred, 01324 shifts (A) left 35 places to restore (A) to the original test value. The second check is performed by 01325, which checks to determine if (A) is equal to the original test value. If (A) is of the correct value, a jump is executed to 01330, which alters the test value by shifting (Q) left by 35 places. Next, Index Jump 01331 causes the cycle to be repeated 33 times.

A peculiar condition exists during the first cycle. Normally, the Threshold Jump instruction 43uv produces a jump to v if u is greater than (A). However, when Threshold Jump 01323 is executed the first time, (A_{71}) is initially in the

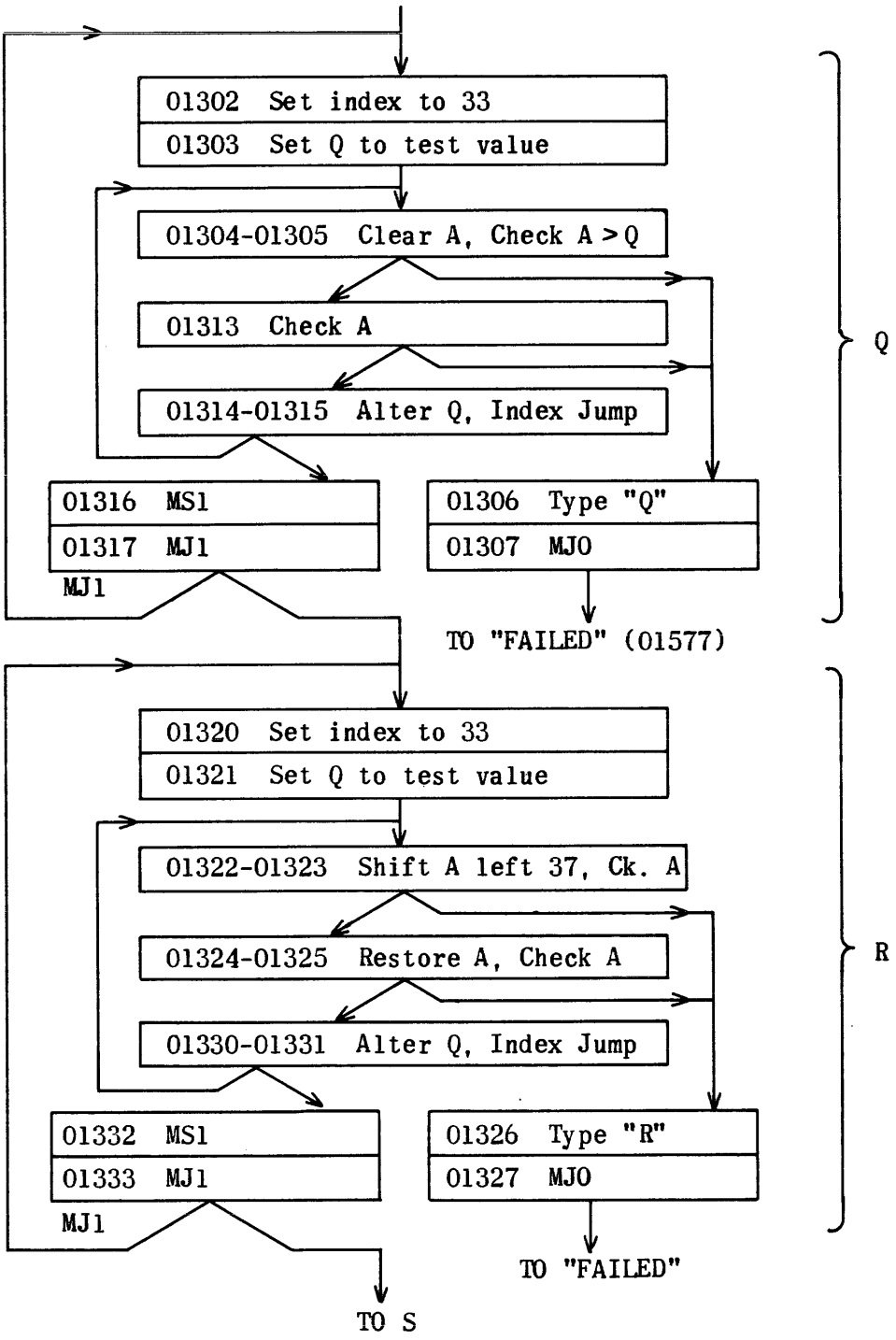

Figure 7. Parts Q and R of Command Test
PX 144

"1" state so that (A) is apparently negative, and thus (Q) is greater than (A). But when (Q) is subtracted from (A), the value of (A_{71}) changes from "1" to "0", so that no jump is executed.

19) TEST S. - Instruction 01334 sets index 01350 to 35. Next, 01335 transmits a test word from 01351 to Q. An indexed cycle starting at 01336, performed 36 times, performs operations on this test word.

At the start of the indexed cycle, 01336 shifts (Q) left once to form a new test word in Q. Next, the u and v portions of (Q) are transmitted to 01352. Next, 01341 forms the bit-by-bit product of an operation code mark and Q in A, which effectively transmits only the first two octal digits of the test word to A. Next, 01342 adds the u and v portions of 01352 to (A) so that the test word is reconstructed in A. For purposes of checking A, the content of A is converted into a 72-bit numerical value by Transmit Positive instruction 01343, and is compared to the original test word value by 01344. If (A) is not equal to the test word, the error termination is executed. If no errors occur, a jump to 01354 is executed. After Index Jump 01354 has caused the test cycle to be repeated 35 times, the test is terminated as usual.

20) TEST T. - This test contains a main indexed cycle performed 36 times, and a subcycle performed 36 times during each main cycle. At the beginning of the test, 01357 sets the main cycle index to 36, and 01360 produces a jump to the start of the main cycle at 01405.

During each performance of the main cycle, 01405 sets the subcycle index to 36, 01406 shifts a test word stored in 01364 left in Q by one place, and Index Jump 01407 causes the subcycle to be performed 36 times. When 1296 subcycles have been completed, the 37th execution of 01407 terminates the test.

During each subcycle, 01367 forms the bit-by-bit product of the test word in Q and the test word in 01364 and transmits the results to 01365. If no errors have occurred, (Q) and 01364 both equal the test word, and the bit-by-bit product of these two values also equals the test word. Next, the test word in Q is complemented and the bit-by-bit product of (Q), and the test word in 01364 is transmitted to 01366. If no errors occur, this leaves 01366 and (A) both zero. Instruction 01372 recomplements (Q) to contain the test word, and 01373 forms the bit-by-bit product of (Q) and the test word in 01365 and adds this product to (A). Because (A) was zero, (A) becomes equal to the test word. For purposes of checking, the test word in A is converted to a 72-bit value by Transmit Positive instruction 01374. Next, Equality Jump 01375 produces a jump to 01400 if no errors have occurred and (A) is equal to the test word. If errors occur, 01376 is executed to start the printing of "T FAILED".

A second check is performed during each subcycle by 01400, 01401, and 01402. Instruction 01400 forms the bit-by-bit product of the test words in Q and in 01365 and of the complement of (Q) and 01366, and transmits the sum of the two products to 01366. The execution of 01400 leaves 01366 equal to the test word. Instruction 01401 subtracts the test word in 01364 from (A). If no errors occur, (A) is zero, and 01403 shifts the test word in Q left by one. If an error occurs, instruction 01402 produces a jump to print "T FAILED".

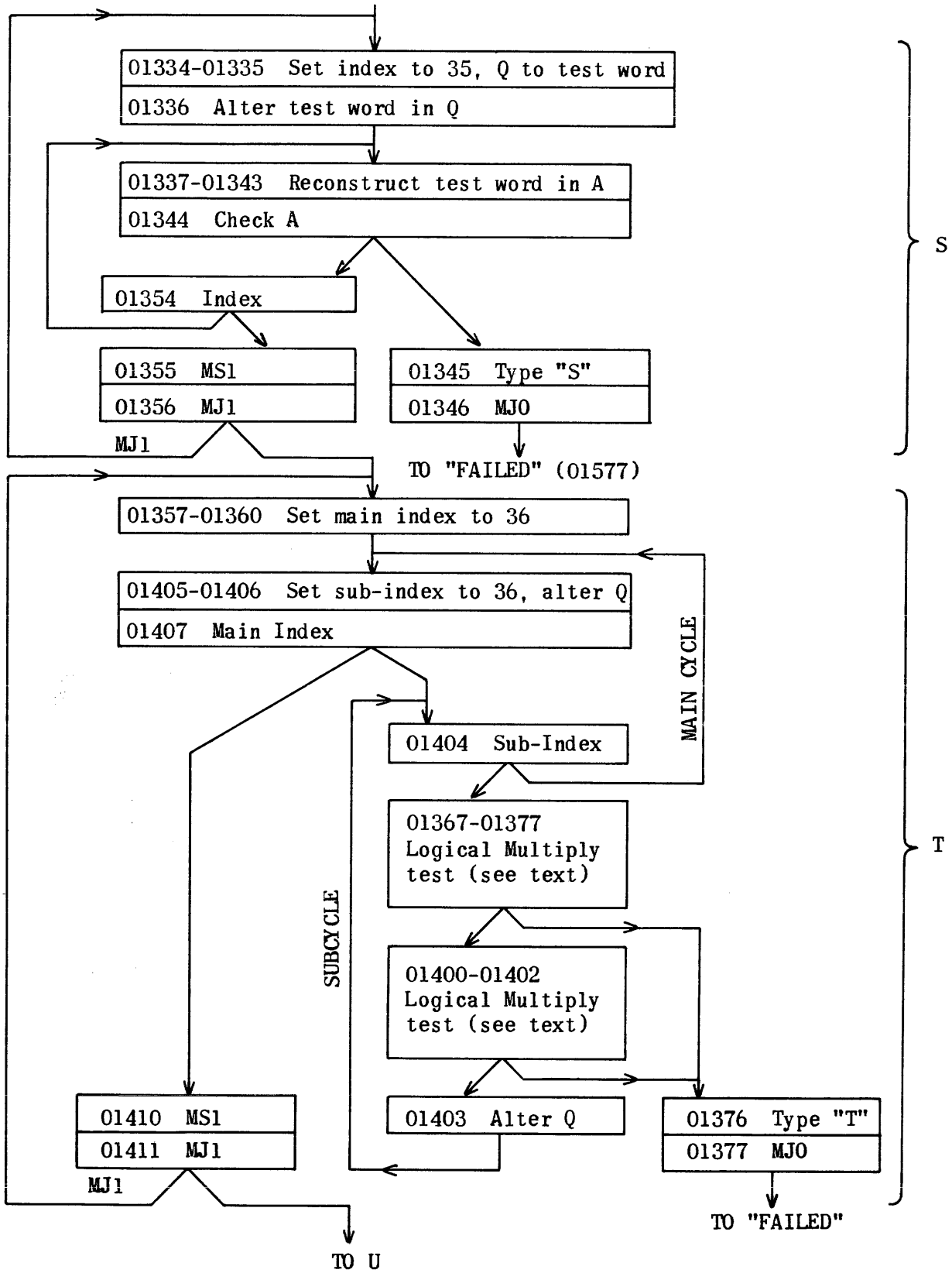

Figure 8. Parts S and T of Command Test
PX 144

21) TEST U. - This test contains a main indexed cycle performed 36 times, and a subcycle performed 36 times, during each main cycle. At the beginning of the test, 01412 sets the main cycle index to 36, and 01413 produces a jump to the start of the main cycle at 01430.

During each performance of the main cycle, 01430 sets the subcycle index to 36, 01431 shifts a test word stored at 01414 to the left in Q by one place so that the next 36 subcycles operate with a new test word, and Index Jump 01432 causes the subcycle to be performed 36 times, When the 1296 subcycles have been completed, the 37th execution of 01432 terminates the test in the usual manner.

During each subcycle, 01420 forms the product of the test word in 01414 and the test word in Q and leaves this product in A. Next, 01421 complements (Q) to set (Q) to the negative of the test word. Instruction 01422 forms a product equal to the negative of the previous product, and adds this product to (A). As a result, if no errors occur, (A) is cleared to zero. If an error occurred, (A) is not zero, and 01423 jumps to start the printing of "U FAILED".

22) TEST V. - This test contains a main indexed cycle performed 36 times, and a subcycle performed 36 times, during each main cycle. At the beginning of the test, 01435 sets the main cycle index to 36, and 01436 produces a jump to the main cycle at 01457.

During each performance of the main cycle, 01457 sets the subcycle index to 36, 01460 shifts a test word T_1 left one place in Q, and Index Jump 01461 causes the subcycle to be performed 36 times. When 1296 subcycles have been completed, the 37th execution of 01461 terminates the test.

Two checks are executed during each subcycle. When either check determines that an error has occurred, instruction 01451 is executed so that "V FAILED" is typed. The checking is performed after operations are executed on two test words T_1 and T_2. Test word T_1, stored in 01442, is altered during each subcycle. Test word T_2, stored in 01443, is not altered. The significant property of T_2 is that it is greater than 36.

Instruction 01445 sets (A) to 36, and 01446 adds the product of the two test words to (A). Next, 01447 divides (A) by T_2, and the dividend is transmitted to 01444. Because T_2 is greater than 36, the dividend becomes equal to T_1, and the remainder in A is equal to 36, if no errors occur. The first check is executed by 01450, which causes 01451 to start the printing of "V FAILED" if an error occurs.

If no errors have occurred up to this point, a jump to 01453 is executed. Instruction 01453 subtracts 36 from the remainder in A. If no errors occur, this leaves zero in A. The second check, performed by 01454, produces a jump to print "V FAILED" if (A) is not zero. If no errors occur, 01455 alters (Q), and 01456 causes the subcycle to be repeated 36 times.

23) TEST W. - This test checks the operation of the Scale Factor (74uv) instruction. Instruction 01464 sets (Q) to 71, and 01465 executes a jump to an indexed cycle starting at 01507. The indexed cycle is executed 71 times.

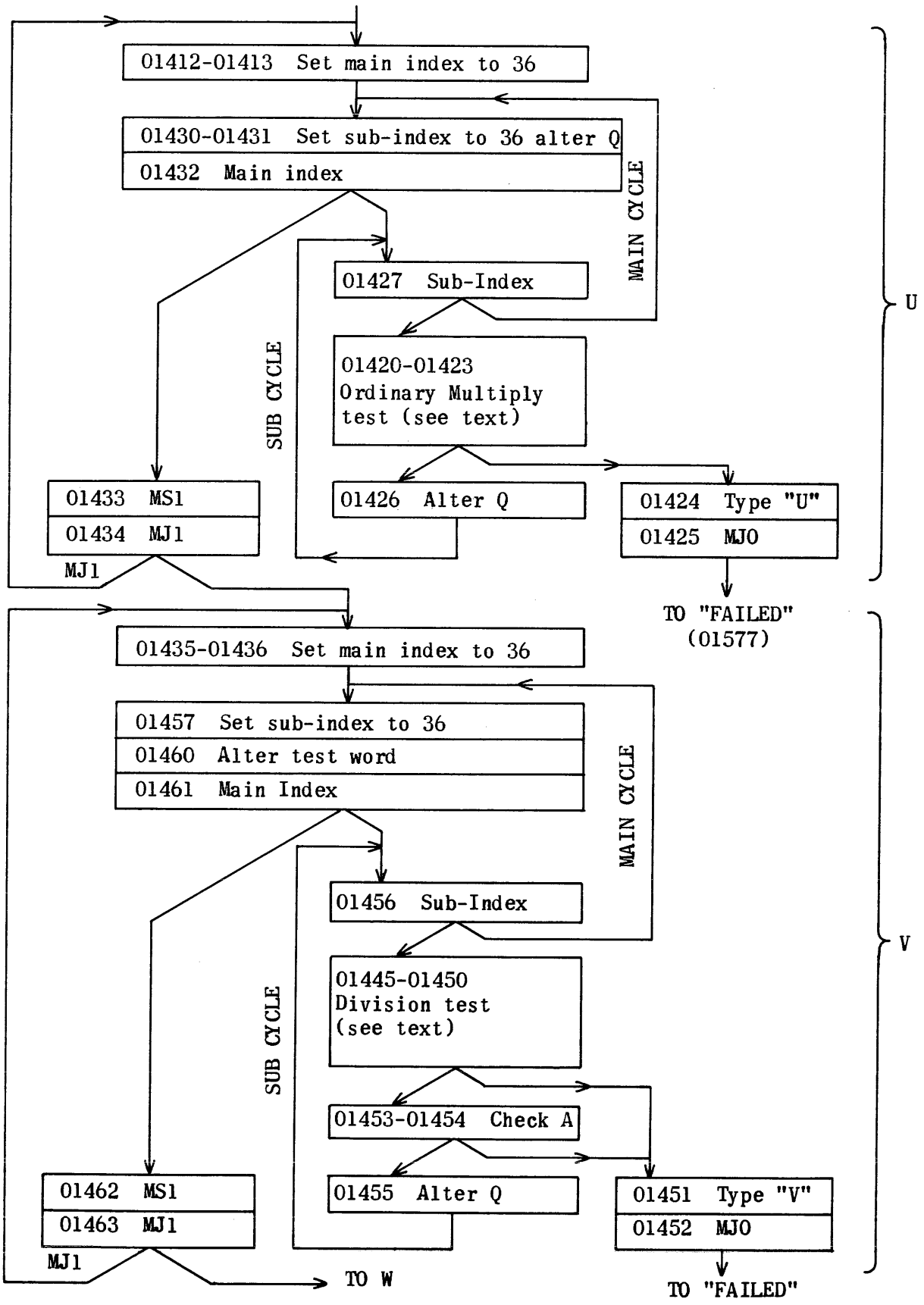

Figure 9. Parts U and V of Command Test
PX 144

During each performance of the indexed cycle, Index Jump instruction 01507 subtracts one from (Q). During the first 71 cycles, 01507 is followed by 01466. Instruction 01466 inserts the current index value n into the next instruction. Next, 01467 adds one to the test value in A and shifts (A) left by n places. Instructions 01470, 01471, 01472, and 01473 store the resulting 72-bit number in addresses 01505 and 01506.

Scale Factor instruction 01474 shifts (A) left until $A_{34} \neq A_{35}$, and inserts the shift count k in the next instruction. This count is the number of places which (A) must be shifted left to restore (A) to its previous condition. The next instruction restores (A) by shifting (A) left k places. Next, 01476 and 01477 subtract the original value of (A), stored in 01505 and 01506, from (A). If no errors occur, (A) becomes zero. Instruction 01500 checks (A), and if (A) is zero, a jump is executed to Index Jump 01507, which causes the cycle to be repeated. The test is terminated as usual.

24) TEST X. - Test X performs the same functions as Test W, except that the test word in A is reduced by one during each cycle, instead of (A) being increased by one.

25) TEST Y. - At the beginning of Test Y, (Q) is zero. Scale Factor instruction 01534 produces a shift count k of 37, because (A) is zero. The first check is performed by 01535, which produces a jump to print "Y FAILED" if (A) is not zero, or to the no-error termination if no errors occurred.

Instruction 01540 sets (A) to 37, then a second check is executed by 01542, If k is not 37, the printing of "Y FAILED" is started. If k is 37, a jump is executed to 01544, to terminate the test.

26) TEST Z. - Instruction 01546 transmits a test word, 43 00000 01551, to A. Next, the repeat condition is established by 01547, which has a jn value of 21551 (octal), and repeated instruction 01550 checks the contents of each consecutive MC address, starting at 00000, for the test word. If no errors occur, execution number 1551 (octal) produces a jump to instruction 01551 and leaves the value j, n-r in Q. Because jn is 21551 (octal) and the number of executions r is 1551 (octal), (Q) is left 20000. Instruction 01551 transmits (Q) to A, and 01552 checks (A) with a constant stored at 01563. If there is an error, the program proceeds to 01533, and the "Z FAILED" sequence is executed.

If there is no error, a jump to 01556 is executed, and this instruction transfers the contents of 01554 to F_2. Instruction 01557 inserts a MJ0 jump to F_1 into MC address 00002, and 01560 alters the v-portion of 01562 so that, if 01561 fails to jump, the "Z FAILED" sequence will be started. If instruction 01561 performs properly, the v-portion of F_1 is set to 01562 and a jump to F_2 is executed. F_2 alters the v-portion of 01562 so that it contains 01570. The next instruction, 00002, is a MJ0 jump to F_1, and F_1 is a MJ0 jump to instruction 01562. Instruction 01562 is a MJ0 jump which, if F_2 has failed to alter the v-portion of 01562, executes a jump to the "Z FAILED" sequence. If the v-portion of 01562 has been altered properly by F_2, a MJ0 jump to 01570 is executed. Instruction 01570 is a MS1 stop which stops the program if MS1 has been selected. If the SELECT STOP 1 button has not been pressed, the program continues to 01571, which is a MJ0 jump to 01607. Test Z is repeated if the

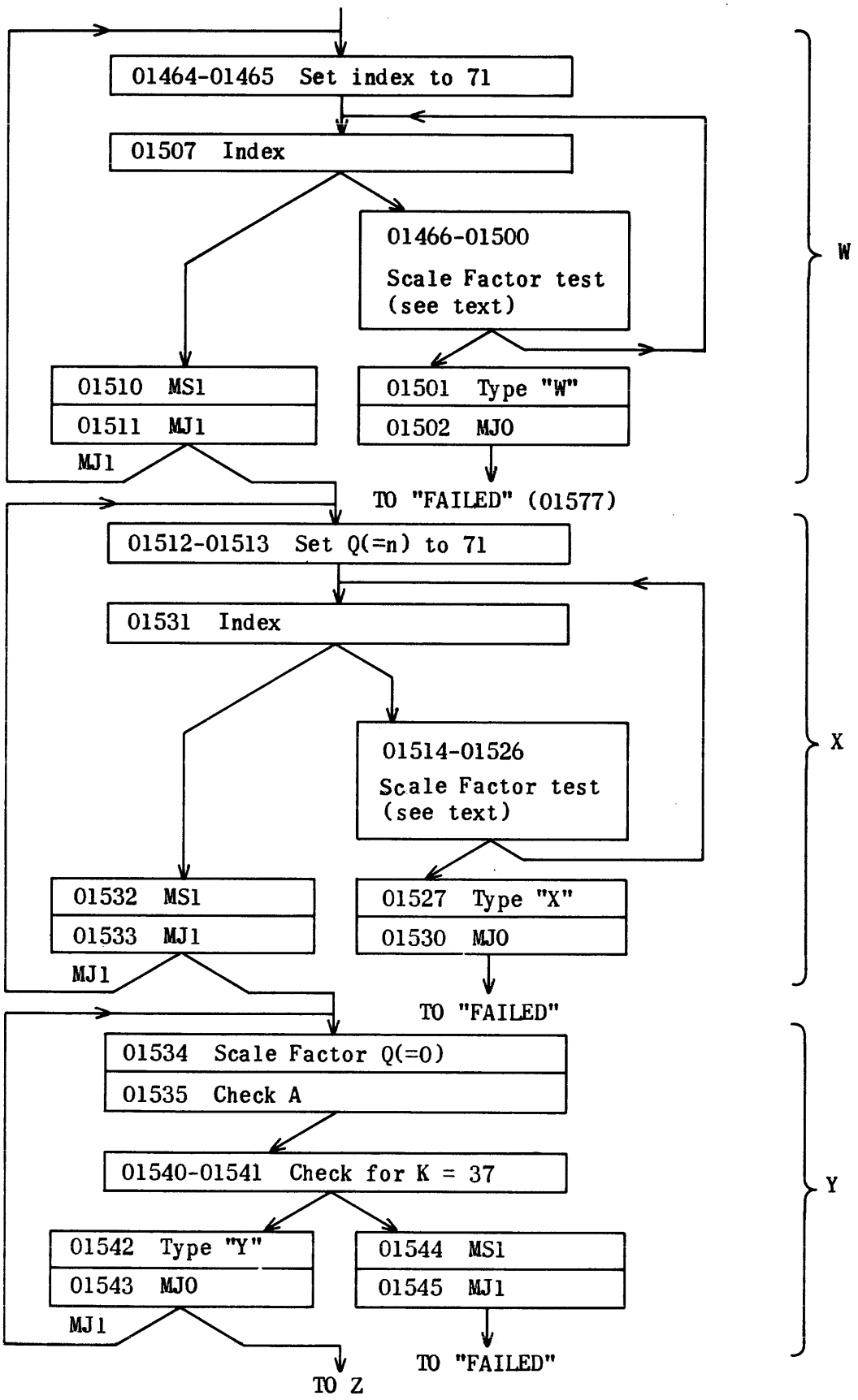

Figure 10. Parts W, X, and Y of Command Test
PX 144

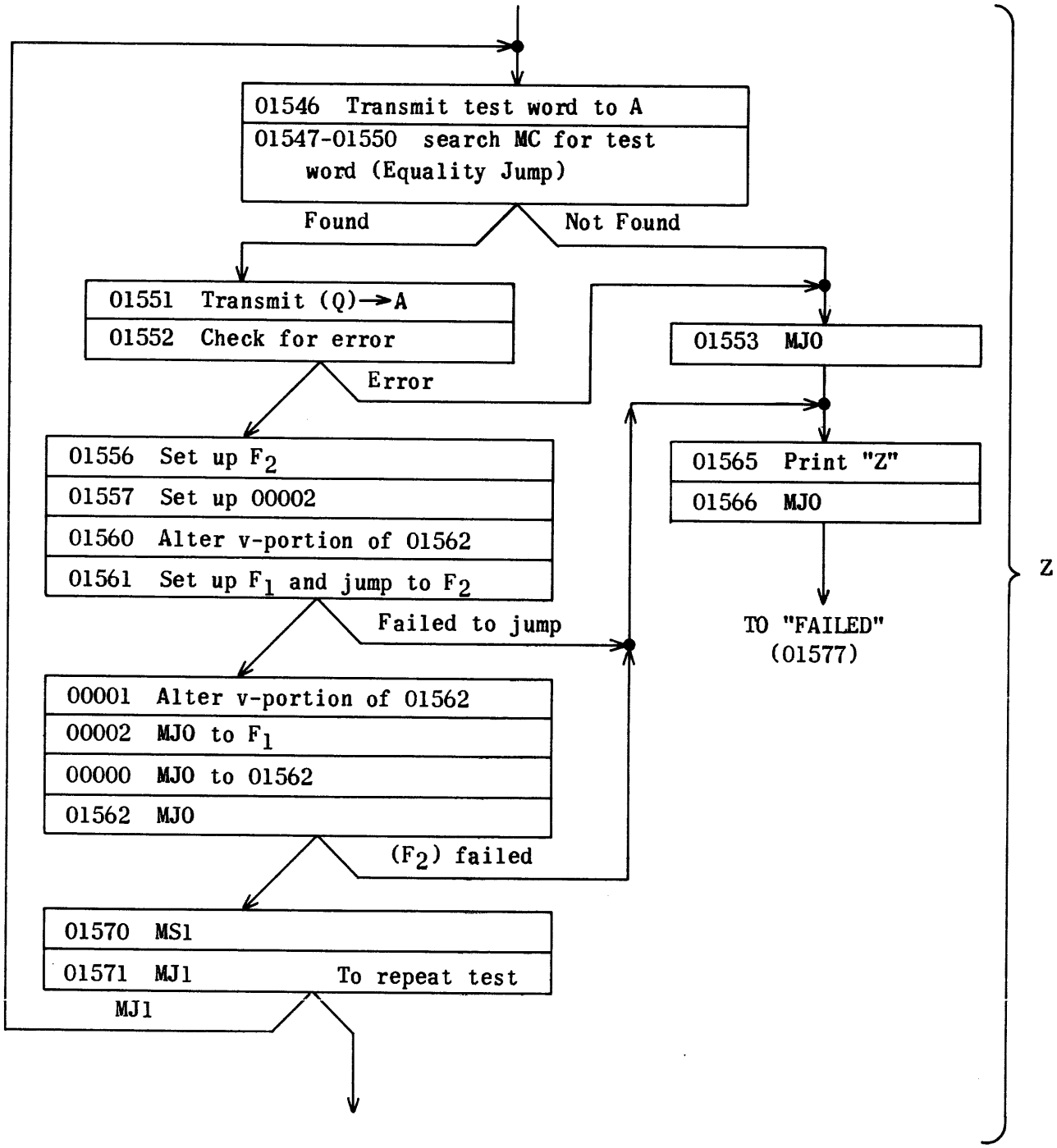

Figure 11. Part Z of Command Test
PX 144

SELECT JUMP 1 button has been pressed. Otherwise, the program continues to instruction 01610 which is Part 22.

27) TEST 22. - This test consists of a main indexed cycle performed 20 times and a distributor controlled sub-cycle performed four times during each main cycle. Instruction 01621 sets the main cycle index to 20, and the next instruction forms a test word and stores it at an MD address.

During the first sub-cycle, the test word is transmitted to A, and a 22 instruction (j=0, k=36, v=A) is performed, thus shifting the test word to A_L and transmitting A_L to A. The first error check is then executed, and, if an error has occurred, a jump is produced to the error termination. If no error occurred, the sequence continues, and a repeat 22 instruction (j=0, k=1, v=Q) is executed 36 times. On each execution A is shifted left one place, and A_L is transmitted to Q. Thus after 36 executions, the test word will be present in both A_L and Q. A "no shift" 22 (j=0, k=0, v= an MC address) is then executed to transmit A_L to MC. The following instruction then transmits the test word at the MC address to A. The second error check is now performed, and A is checked against Q. If no errors occur, the third check is performed and A is checked against the original test word contained in the drum address. If there are no errors, the test word is then complemented and distributor 1 executes a jump to repeat the testing sequence, this time operating on the complemented test word.

After the second sub-cycle the test word is again complemented, and distributor 1 executes a jump to distributor 2 which in turn alters the j and k values of the repeat 22 instruction, and the j value of the no shift 22 instruction then executes a jump to repeat the testing sequence.

On the third sub-cycle, each execution of the repeated 22 instruction now shifts A left two places and transmits A_R rather than A_L to Q. Thus after 36 executions, the test word will have been shifted 72 total places and will be contained in A_R and Q. The no shift 22 then transmits A_R to MC, and the program continues as before. At the end of the third cycle, the test word is again complemented and the fourth cycle executed this time with the complemented test word.

After the fourth cycle, distributor 1 executes a jump to distributor 2, which in turn, restores the original j and k values of the repeat and no shift 22 instructions, then produces a jump to 01653. Instruction 01653 modifies the word forming instruction to produce a new test word for the next cycle, and instruction 01654 reduces the main index by one, then executes a jump to repeat the cycle.

If an error is detected on any of the error checks, a jump is executed to the error termination and "22 FAILED" is printed.

When the main cycle index reaches zero, 01655 is executed to restore the original word forming instruction the remaining instructions are an MS1 to stop the test, an MJ1 to repeat the test and an MJ0 to the no error termination.

28) NO-ERROR TERMINATION. - If no errors occur during any of the tests, the test is repeated if SELECT JUMP 1 is selected, or the next test is

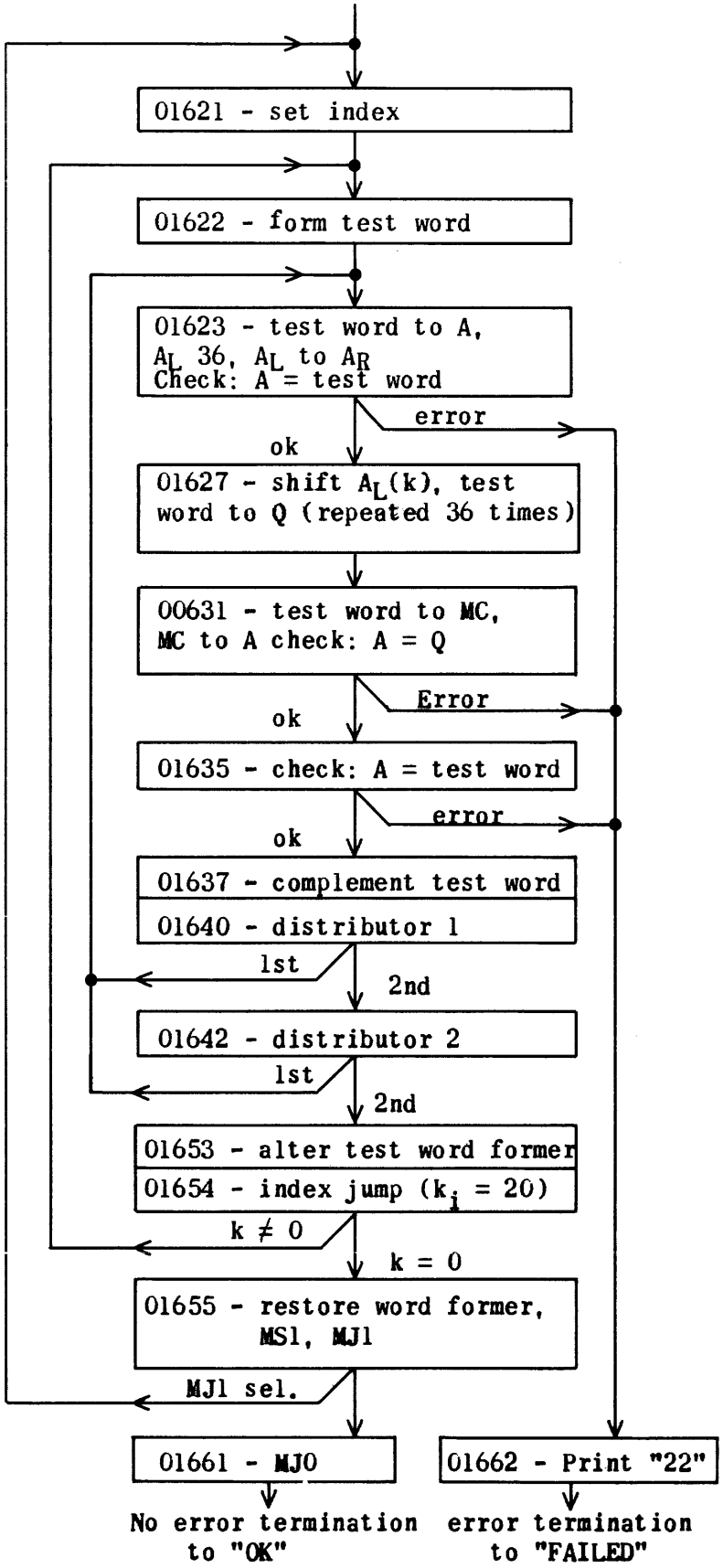

Figure 12. Part "22" of Command Test
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executed if the jump is not selected. At the end of Test Z, the entire test routine is concluded by execution of 01572 through 01576. Instruction 01572 produces a stop if SELECT STOP 2 is selected, and 01573 produces a jump to Test A if SELECT JUMP 2 is selected. If the latter jump is not selected, 01574 and 01575 type "OK" and 01576 produces a stop. The entire test is restarted when START is pressed.

29) ERROR TERMINATION. - If an error occurred during any test, a Manually Selective Jump 0 instruction produces a jump to 01577. Instructions 01577 through 01605 type "FAILED", and 01606 produces a stop if SELECT STOP 3 has been selected. When START is pressed, the entire test program is restarted at address 01000.

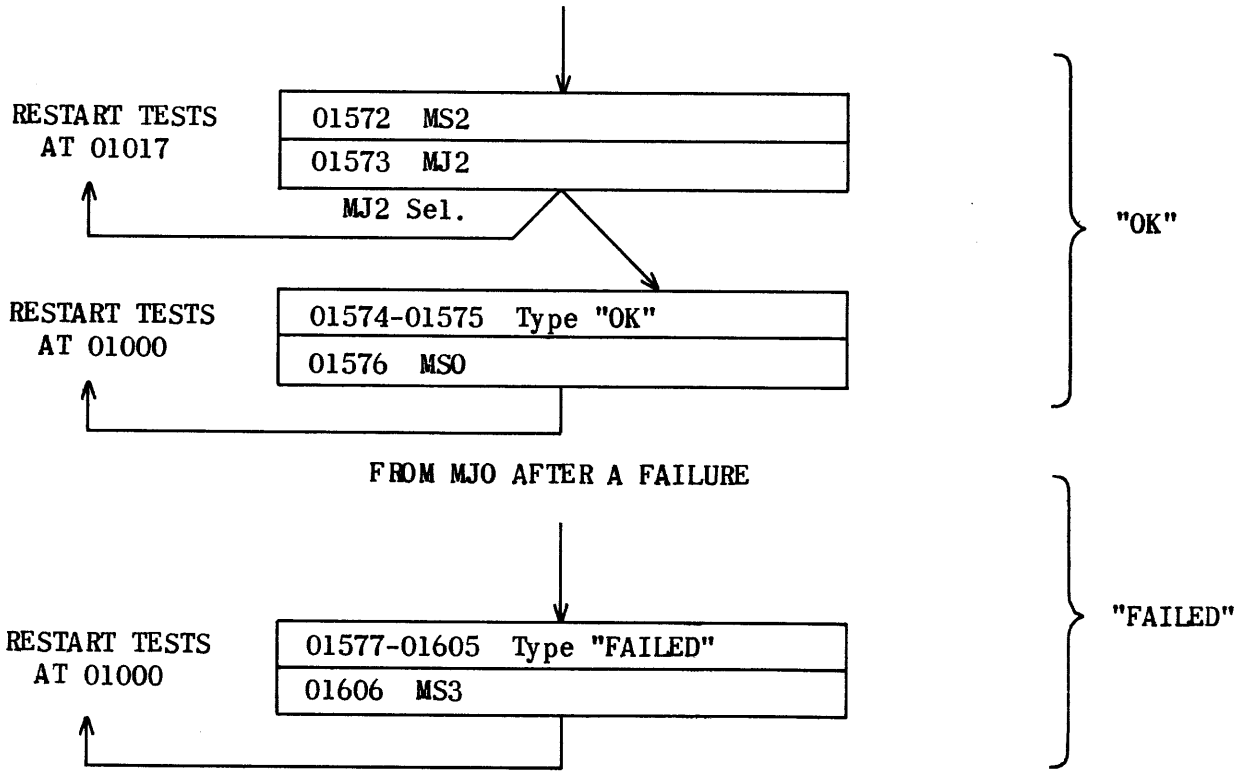

Figure 13. Parts "OK" and "FAILED" of Command Test
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TABLE 1. LONG COMMAND TEST - FLEX CODE

PROGRAM: Long Command Test

DESCRIPTION: Tests all computer instructions except those involving external equipments. Manual selections as follows: MS1 to stop at end of each part; MJ1 to repeat last part; MS2 to stop at end of entire test; MJ2 to repeat entire test; MS3 to stop after a failure.

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
46000	11	46001	00000	Store jump instr. in F_1
46001	45	00000	46002	Jump to 46002
46002	75	30667	01000	Block Transfer from MD Storage to High Speed Storage
46003	11	46004	01000	
46004 thru 41072				See 01000 thru 01666
				Type Heading
01000	61	00000	01046	Carriage return
01001	61	00000	01027	Shift up
01002	61	00000	01036	C
01003	61	00000	01241	O
01004	61	00000	01200	M
01005	61	00000	01200	M
01006	61	00000	01020	A
01007	61	00000	01217	N
01010	61	00000	01052	D
01011	61	00000	01160	Space
01012	61	00000	01370	T
01013	61	00000	01061	E
01014	61	00000	01335	S
01015	61	00000	01370	T

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01016	61	00000	01160	Space
01017	23	31000	31000	Clear Q and A
				Test A (A = 0, Q = 0)
01020	11	31000	32030	Transmit 36 zeros to A
01021	47	01022	01024	Check A
01022	61	00000	01020	Error termination
01023	45	00000	01577	
01024	56	10000	01025	No-error termination
01025	45	10000	01020	
				Test B (A = 0, Q = 0)
01026	13	32000	31023	Transmit 36 ones to Q
01027	11	31000	32047	Transmit (Q) to A
01030	47	01031	01033	Check A
01031	61	00000	01026	Error termination
01032	45	00000	01577	
01033	56	10000	01034	No-error termination
01034	45	10000	01027	
				Test C (A = 0)
01035	41	32000	01044	Subtract 1 from A
01036	13	32000	31016	Set Q to +1
01037	11	01042	01047	Transmit MSO instr. into 01047
01040	37	01047	01046	Jump to 01046-01047, return to 01041
01041	43	31000	01043	Check A, if A = +1 jump to 01043
01042	45	00000	01044	Jump to error termination

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01043	41	32000	01050	Subtract 1 from A, jump to 01050
01044	61	00000	01036	} Error termination
01045	45	00000	01577	
01046	13	32000	32045	Complement A
01047	45	00000	01041	Jump to 01041
01050	56	10000	01051	} No-error termination
01051	45	10000	01035	
				Test D (A = 0, Q = +1)
01052	35	31000	32022	} Add 36 ones to A
01053	44	01054	01052	
01054	47	01055	01057	Check for A = 0
01055	61	00000	01052	} Error termination
01056	45	00000	01577	
01057	56	10000	01060	} No-error termination
01060	45	10000	01052	
				Test E (A = 0, Q = +1)
01061	13	31000	31020	Set Q to -1
01062	36	31000	32014	} Subtract 36 ones from A
01063	44	01062	01064	
01064	47	01065	01067	Check A
01065	61	00000	01061	} Error termination
01066	45	00000	01577	
01067	56	10000	01070	} No-error termination
01070	45	10000	01062	

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
				Test F (A = 0, Q = 1)
01071	35	31000	32026	Add 36 zeros to A
01072	44	01071	01073	
01073	47	01074	01076	Check A
01074	61	00000	01071	Error termination
01075	45	00000	01577	
01076	56	10000	01077	No-error termination
01077	45	10000	01071	
				Test G (A = 0, Q = -1)
01100	13	31000	31013	Set Q = +1
01101	36	31000	32005	Subtract 36 ones from A
01102	44	01103	01101	
01103	47	01104	01106	Check A
01104	61	00000	01100	Error termination
01105	45	00000	01577	
01106	56	10000	01107	No-error termination
01107	45	10000	01101	
				Test H (A = 0, Q = +1)
01110	32	31000	00001	Split-add 71 ones to A
01111	46	01112	01110	
01112	32	31000	00000	Add +1 to A
01113	47	01114	01116	Check A
01114	61	00000	01101	Error termination
01115	45	00000	01577	

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01116	56	10000	01117	No-error termination
01117	45	10000	01110	
				Test I (A = 0, Q = +1)
01120	34	31000	00001	Split-subtract 71 ones from A
01121	46	01120	01122	
01122	34	31000	00000	Subtract 1 from A
01123	47	01124	01126	Check A
01124	61	00000	01062	Error termination
01125	45	00000	01577	
01126	56	10000	01127	No-error termination
01127	45	10000	01120	
				Test J (A = 0, Q = +1)
01130	13	32000	31032	Set Q to all ones
01131	32	31000	00022	Insert 18 ones in A_L
01132	31	31000	00044	Clear A, form 36 ones in A_L
01133	32	31000	00000	Add 36 ones to A_R
01134	47	01135	01137	Check A
01135	61	00000	01130	Error termination
01136	45	00000	01577	
01137	56	10000	01140	No-error termination
01140	45	10000	01130	
				Test K (A = 0, Q = -0)
01141	32	31000	00022	Enter 18 ones in A_L
01142	33	31000	00044	Clear A, enter 36 ones in A_L

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01143	34	31000	00000	Subtract 36 ones from A_R
01144	47	01145	01147	Check A
01145	61	00000	01152	} Error termination
01146	45	00000	01577	
01147	56	10000	01150	} No-error termination
01150	45	10000	01141	
				Test L (A = 0)
01151	11	01171	01172	Set n (index) to 4096
01152	11	01172	31036	Store n in Q
01153	54	31000	00111	} Form -n in A
01154	54	32000	00107	
01155	36	31000	32011	
01156	55	32000	00045	} Form -n in A
01157	55	31000	00043	
01160	36	31000	31004	
01161	54	31000	00111	} Form +n in A
01162	54	32000	00107	
01163	36	31000	32000	
01164	55	32000	00045	} Form +n in A
01165	55	31000	00043	
01166	36	31000	31000	
01167	34	01172	00000	Subtract +n from A (to clear A)
01170	47	01173	01175	Check A, jump to 01175 if OK
01171	00	00000	10000	Constant = 4096 dec.

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01172	00	00000	00000	Stores index value = n
01173	61	00000	01155	} Error termination
01174	45	00000	01577	
01175	41	01172	01152	Index n, jump to 01152
01176	56	10000	01177	} No-error termination
01177	45	10000	01151	
				Test M (A = 0)
01200	11	01212	31007	Set Q to 4096
01201	12	31000	32000	Transmit Q (=n) to A
01202	43	31000	01205	Check A, jump to 01205 if A = Q
01203	61	00000	01200	} Error termination
01204	45	00000	01577	
01205	13	32000	32000	Set A to -n
01206	43	31000	01203	Check A, jump to 01203 if A = Q
01207	12	32000	32000	Set A to +n
01210	43	31000	01213	Check A, jump to 01213 if A = Q
01211	45	00000	01203	Jump to error termination
01212	00	00000	10000	Constant = 4096
01213	41	31000	01214	Subtract 1 from Q
01214	41	32000	01201	Jump (4096 times) to 01201
01215	56	10000	01216	} No-error termination
01216	45	10000	01200	
				Test N (A = -1, Q = -1)
01217	13	32000	31006	Set Q to +1

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01220	11	01224	01225	Set index to 4096
01221	23	32000	32000	Clear A
01222	75	00014	01226	Form sum (see text) in A
01223	32	01225	00006	
01224	00	00000	10000	Constant = 4096
01225	00	00000	00000	Stores index
01226	35	31000	32000	Alternately add and subtract in A
01227	36	31000	32000	
01230	44	01231	01226	
01231	75	00014	01233	Subtract sum (see text) from A
01232	34	01225	00006	
01233	47	01234	01236	Check A
01234	61	00000	01217	Error termination
01235	45	00000	01577	
01236	41	01225	01221	Jump 4096 times to 01221
01237	56	10000	01240	No-error termination
01240	45	10000	01220	
				<u>Test 0</u> (A = 0)
01241	11	01252	31003	Set Q (=n) to 4096
01242	11	31000	01253	Store n
01243	13	31000	01254	Store -n
01244	23	01253	01255	Store n-1
01245	21	01254	01255	Store 1-n
01246	13	01254	32000	Set A to n-1

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01247	43	01253	01256	Check A against (01253)
01250	61	00000	01241	Error termination
01251	45	00000	01577	
01252	00	00000	10000	Constant, = 4096
01253	77	77777	77776	Constant = -1
01254	00	00000	00001	Constant = 1
01255	00	00000	00001	Constant = 1
01256	41	31000	01242	Jump (4096 times) to 01242
01257	56	10000	01260	No-error termination
01260	45	10000	01241	
				Test P
01261	23	31000	31015	Clear A and Q
01262	27	31000	31000	Form bit-by-bit sum of Q + Q in A
01263	35	31000	32000	Add Q to A
01264	47	01265	01267	Check A
01265	61	00000	01261	Error termination
01266	45	00000	01577	
01267	13	31000	31000	Set Q to 36 ones
01270	27	32000	31000	Form bit-by-bit sum of A + Q in A
01271	54	32000	00044	Shift A left 36
01272	32	31000	00000	Add Q to A
01273	47	01265	01274	Check A
01274	31	31000	00044	Enter 36 ones in A_L
01275	27	32000	31000	Form 72 ones in A

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01276	47	01277	01265	Check A, clear A to 72 zeros
01277	47	01265	01300	Check A
01300	56	10000	01301	No-error termination
01301	45	10000	01261	
				Test Q
01302	11	01311	01312	Set index to 33
01303	11	01310	31035	Set Q to test value
01304	23	32000	32000	Clear A
01305	42	31000	01313	Check A $\leq$ Q
01306	61	00000	01303	Error termination
01307	45	00000	01577	
01310	20	00000	00000	Test value, = 2×8^{11}
01311	00	00000	00041	Constant, = 33
01312	00	00000	00000	Storage for index
01313	47	01306	01314	Check A $\neq$ 0
01314	55	31000	00043	Alter test value in Q
01315	41	01312	01304	Jump (33 times) to 01304
01316	56	10000	01317	No-error termination
01317	45	10000	01302	
				Test R
01320	11	01311	01312	Set index to 33
01321	11	01310	31012	Set Q to test value
01322	31	01310	00045	Shift A left 37
01323	42	31000	01326	Check A

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01324	54	32000	00043	Restore A to test value
01325	43	01310	01330	Check A
01326	61	00000	01321	Error termination
01327	45	00000	01577	
01330	55	31000	00043	Shift Q left 35
01331	41	01312	01322	Jump to 01322 (33 times)
01332	56	10000	01333	No-error termination
01333	45	10000	01320	
01334	11	01347	01350	Set index to 35
01335	11	01351	31024	Set Q to test word
01336	55	31000	00001	Shift Q left 1
01337	16	31000	01352	Store u and v of test word
01340	15	31000	01352	
01341	51	01353	32000	Isolate operation code in A
01342	35	01352	32000	Reconstruct test word in A (A_R = Q)
01343	11	32000	32000	Convert test word into 72-bit extension
01344	43	31000	01354	Check A against (01351)
01345	61	00000	01335	Error termination
01346	45	00000	01577	
01347	00	00000	00043	Constant, = 35
01350	00	00000	00000	Storage for index
01351	77	77565	20000	Test word
01352	00	77565	32000	Temporary Storage
01353	77	00000	00000	Operation code mask

TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01354	41	01350	01336	Jump (35 times) to 01336
01355	56	10000	01356	No-error termination
01356	45	10000	01334	
				Test T
01357	11	01361	01362	Set main cycle index to 36
01360	45	00000	01405	Jump to 01405
01361	00	00000	00044	Constant, = 36
01362	00	00000	00000	Storage for main cycle index
01363	00	00000	00044	Sub-cycle index storage
01364	00	07777	52520	Test word
01365	00	01777	60000	Test word
01366	00	03777	65250	Test word
01367	51	01364	01365	Form bit-by-bit product #1
01370	13	31000	31001	Complement Q
01371	51	01364	01366	Form bit-by-bit product #2
01372	13	31000	31000	Complement Q
01373	52	01365	32000	Form bit-by-bit product #3 in A
01374	11	32000	32000	Convert A_L to 72-bit extension
01375	43	01364	01400	Check A
01376	61	00000	01370	Error Termination
01377	45	00000	01577	
01400	53	01365	01366	Form bit-by-bit product #4
01401	34	01364	00000	Subtract test word from A
01402	47	01376	01403	Check A

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TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	*	▼	ORIGINAL DRUM CONTENT
01403	55	31000	00001	Alter test word in Q
01404	41	01363	01367	Jump 36 times to 01367
01405	11	01361	01363	Set sub-cycle index to 36
01406	55	01364	00001	Shift test word left 1 to Q
01407	41	01362	01404	Jump 36 times to 01404
01410	56	10000	01411	} No-error termination
01411	45	10000	01357	
				Test U
01412	11	01415	01416	Set main index to 36
01413	45	00000	01430	Jump to 01430
01414	12	77774	00013	Test word
01415	00	00000	00044	Constant, = 36
01416	00	00000	00000	Store main index
01417	00	00000	00044	Store sub-cycle index
01420	71	31000	01414	Form product #1
01421	13	31000	31034	Complement Q
01422	72	31000	01414	Form neg. of prod. #1, subtr. from A
01423	47	01424	01426	Check A
01424	61	00000	01421	} Error termination
01425	45	00000	01577	
01426	55	31000	00001	Shift Q left 1
01427	41	01417	01420	Jump (36 times) to 01420
01430	11	01415	01417	Set sub-cycle index to 36
01431	55	01414	00001	Alter test word in Q

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TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01432	41	01416	01427	Jump (36 times) to 01427
01433	56	10000	01434	} No-error termination
01434	45	10000	01412	}
				Test V
01435	11	01437	01440	Set main index to 36
01436	45	00000	01457	Jump to 01457
01437	00	00000	00044	Constant, = 36
01440	00	00000	00000	Main index
01441	00	00000	00044	Sub index
01442	37	77600	00525	Test word T_1
01443	67	60210	14176	Test word T_2
01444	00	00000	00000	Quotient
01445	11	01437	32017	Set A to 36
01446	72	01442	01443	$(T_1T_2 + 36)$ A
01447	73	01443	01444	$(T_1T_2 + 36) / T_2$ (01444)
01450	43	01437	01453	Check remainder
01451	61	00000	01445	} Error termination
01452	45	00000	01577	}
01453	23	01444	01442	Subtract T_1 from quotient
01454	47	01451	01455	Check for A = 0
01455	55	01443	00001	Alter T_2, shift 1 place
01456	41	01441	01445	Jump (36 times) to 01445
01457	11	01437	01441	Set sub-cycle index to 36
01460	55	01442	00001	Shift T_1 left 1 in Q

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TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01461	41	01440	01456	Jump to sub-cycle 36 times
01462	56	10000	01463	No-error termination
01463	45	10000	01435	
				Test W
01464	11	01504	31031	Set main index to 71
01465	45	00000	01507	Jump to 01507
01466	16	31000	01467	Insert index n in NI
01467	31	01503	00000	A + 1
01470	54	32000	00044	Store 71-bit test value
01471	11	32000	01505	Store 71-bit test value
01472	54	32000	00044	
01473	11	32000	01506	
01474	74	32000	01475	Scale factor A, insert k in NI
01475	54	32000	00046	Shift A left 38 places
01476	34	01506	00044	Subtract 71-bit value from A
01477	34	01505	00000	
01500	47	01501	01507	Check A = 0
01501	61	00000	01464	Error termination
01502	45	00000	01577	
01503	00	00000	00001	Constant, = 1
01504	00	00000	00107	Constant, = 71
01505	77	77777	77777	Storage for 72-bit test value
01506	77	77777	77776	
01507	41	31000	01466	Jump (71 times) to 01466

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TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01510	56	10000	01511	} No-error termination
01511	45	10000	01464	
				Test X
01512	11	01504	31027	Set Q to 71
01513	45	00000	01531	Jump to 01531
01514	16	32000	01515	Insert index n in NI
01515	33	01503	00000	A-1
01516	54	32000	00044	} Store 72-bit test value
01517	11	32000	01505	
01520	54	32000	00044	} Store 72-bit test value
01521	11	32000	01506	
01522	74	32000	01523	Scale-factor A, insert k in NI
01523	54	32000	00046	Shift A left k
01524	34	01506	00044	} Subtract 72-bit value from A
01525	34	01505	00000	
01526	47	01527	01531	Check for A = 0
01527	61	00000	01512	} Error termination
01530	45	00000	01577	
01531	41	31000	01514	Jump (71 times) to 01514
01532	56	10000	01533	} No-error termination
01533	45	10000	01512	
				Test Y (Q = 0)
01534	74	31002	01537	Scale-factor Q, store k
01535	47	01542	01540	Check for A = 0

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TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01536	00	00000	00045	Constant, = 37
01537	00	00000	00045	Scale factor shift count
01540	11	01536	32025	Set A to 37
01541	43	01537	01544	Check for k = 37
01542	61	00000	01540	} Error termination
01543	45	00000	01577	
01544	56	10000	01545	} No-error termination
01545	45	10000	01534	
				Test Z
01546	11	01550	32021	Set A to test word
01547	75	21551	01553	} Search contents of MC for test word
01550	43	00000	01551	
01551	11	31000	32000	Q → A
01552	43	01563	01556	Check A = 32000 (octal)
01553	45	00000	01565	MJO jump to "Z FAILED" sequence
01554	16	01564	01562	Constant: inserted in F_2
01555	45	00000	00000	MJO jump to F_1
01556	11	01554	00001	Set up F_2
01557	11	01555	00002	Set up 00002
01560	11	01553	01562	Alter v-portion of 01562
01561	14	01565	01565	Set up F_1
01562	45	00000	01570	MJO jump to 01570
01563	00	00000	20000	Constant
01564	00	00000	01570	Constant

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TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01565	61	00000	01546	} Error termination
01566	45	00000	01577	
01567	45	00000	01565	MJ0 jump to "Z FAILED" if PAK does not clear on MP1
01570	56	10000	01571	} No-error termination
01571	45	00000	01607	
				Conclude Test
01572	56	20000	01573	MS2
01573	45	20000	01017	MJ2, restart at Test A
01574	61	00000	01241	0
01575	61	00000	01152	k
01576	56	00000	01000	Stop, restart entire routine
				Type failure
01577	61	00000	01160	space
01600	61	00000	01071	F
01601	61	00000	01020	A
01602	61	00000	01062	I
01603	61	00000	01155	L
01604	61	00000	01061	E
01605	61	00000	01052	D
01606	56	30000	01000	MS3, restart entire routine
01607	45	10000	01546	No-error termination (Test Z)
				Test 22
01610	45	00000	01621	Jump to start
01611	25	25252	52525	Test word

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TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	u	v	ORIGINAL DRUM CONTENT
01612	00	10002	00000	} Altering addresses
01613	00	00001	01641	
01614	00	10000	01643	
01615	00	00000	00001	Constant
01616	00	00000	00023	Index
01617	00	00000	00000	Store for index
01620	25	25252	52525	Test word
01621	11	01616	01617	Set index
01622	54	01611	00000	Form test word
01623	11	01611	32000	Test word $\rightarrow$ A
01624	22	00044	32074	$A_R \rightarrow A_L$, $A_L \rightarrow A$
01625	43	01611	01627	Check if A = test word
01626	45	00000	01662	Error jump
01627	75	00044	01631	} $A_R \rightarrow A_L \rightarrow Q$ ($A_R \rightarrow A_R \rightarrow Q$)
01630	22	00001	31057	
01631	22	00000	01667	$A_L \rightarrow$ M.C. ($A_R \rightarrow$ M.C.)
01632	11	01667	32047	M.C. $\rightarrow$ A
01633	43	31000	01635	Check if A = Q
01634	45	00000	01662	Error jump
01635	43	01611	01637	Check if A = test word
01636	45	00000	01662	Error jump
01637	13	01611	01611	Complement test word
01640	45	00000	01641	Jump around 1st RJ every second time through
01641	37	01640	01623	Repeat test with complement test word

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TABLE 1. LONG COMMAND TEST - FLEX CODE (Cont.)

ADDRESS	OP-CODE	▪	▾	ORIGINAL DRUM CONTENT
01642	45	00000	01643	Jump around 2nd RJ every 4th time through
01643	15	01612	01630	Alter j and k of repeated 22 instruction
01644	15	01614	01631	Alter j of no shift 22 instruction
01645	16	01613	01640	Restore jump to 1st RJ
01646	37	01642	01623	Repeat test for new j and k
01647	15	01613	01630	Restore j and k in repeated 22 instructio
01650	15	01615	01631	Restore j in no shift 22 instruction
01651	16	01613	01640	Restore jump to 1st RJ
01652	16	01614	01642	Restore jump to 2nd RJ
01653	21	01622	01615	Add 1 to shift of test word Former
01654	41	01617	01622	Repeat test with new test word (20 times)
01655	11	01620	01611	Restore Test word
01656	16	01612	01622	Restore test word Former
01657	56	10000	01660	
01660	45	10000	01621	No-error termination
01661	45	00000	01572	
01662	61	00000	01630	
01663	61	00000	01624	
01664	61	00000	01624	Error termination
01665	61	00000	01632	
01666	45	00000	01577	

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TABLE 2. SHORT COMMAND TEST

ADDRESS	OP-CODE	■	▼	ORIGINAL DRUM CONTENT
46700	11	46001	00000	Store jump instruction in F_1
46701	75	30647	46710	Block transfer test from M.D. to High speed storage
46702	11	46023	01017	
46703 thru 46726				See 01017 thru 01042
01017	45	00000	01017	Constants and Modifying instructions
01020	00	00000	00100	
01021	00	00000	00010	
01022	56	20000	01017	
01023	56	30000	01017	
01024	11	46703	01000	Modify starting address
01025	11	46706	01661	Modify end jumpout
01026	11	46707	01577	Modify error jumpout
01027	11	46704	01171	Modify constants
01030	11	46704	01212	
01031	11	46704	01224	
01032	11	46704	01252	
01033	11	46705	01361	
01034	11	46705	01415	
01035	11	46705	01437	
01036	45	00000	01017	Jump to start test

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QUAK-POOF TEST

1. GENERAL

The computer instructions are tested under single operation, according to numerical sequence as much as possible. Then most of them are tested under repeated conditions.

The tests are labelled with the operation code of the instruction being tested, followed by a single or double letter designator, such as 11g or 71cc. The letters following the operation code serve to identify one portion of a test on a particular operation code from another. For instance, the first test on the 71 instruction is 71a, then 71b, and so on through 71z, starting over at this point to 71aa. This is done to keep individual portions of a test as small as possible and helps in locating the exact point of failure when this occurs. From a trouble-shooting viewpoint, this is ideal. In the tests concerned with repeated conditions of an instruction, the label is preceded by a small r, such as r32c and r71a.

The POOF portion of this test is the SHORT COMMAND TEST, which must be loaded onto the drum in order to run QUAK-POOF.

2. STOPS AND JUMPS

With no jumps or stops selected, the SHORT COMMAND TEST is block transferred to MC, altered to return to QUAK, and also run. A bar is printed at the conclusion of each test run of QUAK-POOF. The COMMAND TEST must therefore be loaded on the drum to run QUAK-POOF.

STOPS AND JUMPS

MS - 0	None in test.
MS - 1	Stop before error type-out.
MS - 2	Stop after completing QUAK.
MS - 3	Stop after error type-out.
MJ - 0	Jump to start. Jump to POOF after completing QUAK.
MJ - 1	None in test.
MJ - 2	None in test.
MJ - 3	Jump to repeat QUAK only.

3. ERROR TYPE-OUT

The Interpret instruction (IPxx) is used throughout the test for entrance to the ERROR TYPE-OUT subroutine. Since the u and v portions of the Interpret instruction word have no bearing on its function, they are used to store the codes for each type-out. The Interpret instruction stores y + 1 in the v portion of (F_1) and takes (F_2) as the next instruction. In F_2 is a MS-1 which effectively jumps into the TYPE-OUT subroutine. If a MS-1 is selected, the computer stops before typing the test that failed.

The subroutine first stores (A_L) and (A_R). (Q) is not affected by the subsequent operation. The Interpret instruction that caused entrance to the routine is brought up to A where it is shifted, printed, and deleted until (A) = 0. At this time (A_L) and (A_R) are restored. A MS-3 instruction jumps to F_1 which resumes the test at y + 1. With a 3 stop selected, the computer stops after ERROR TYPE-OUT.

Also, it is possible to perform a failing test repeatedly by modifying, in high-speed storage, the v portion of the MS-3 instruction. By making it the beginning address of the failing test, instead of returning to y + 1 by way of (F_1), the MS-3 instruction jumps to re-run the test. In order to restore program to normal, block transfer from drum again or manually insert F_1 into the v portion of the MS-3 instruction.

4. CONVERTING DRUM TO MC ADDRESSES

To convert test addresses from drum to MC, subtract 60000 from each address location.

5. THEORY OF THE TEST

a. GENERAL. - Starting at 60000, a jump to 64466, accomplishes the block transfer of QUAK. Then QUAK is printed. Providing no jumps or stops have been selected, POOF is printed also, and a jump to 00210 starts the QUAK test. After the test has run, the computer may stop or repeat QUAK if selected; otherwise, at this point, the SHORT COMMAND TEST is transferred to high-speed storage and modified to return to QUAK. If the SHORT COMMAND TEST is completed, a bar is printed and a new block transfer of QUAK is accomplished.

If a failure occurs during QUAK, the test label is typed and the test resumed from that point. If a failure occurs during the SHORT COMMAND TEST, the letter of the test having failed is printed and the SHORT COMMAND TEST is started over from the beginning.

b. THE QUAK TEST. - The 11 and 43 codes are used extensively in the testing of all other instructions. Therefore, the first series of tests is concerned with insuring the operation of those two instructions. After this, the tests are performed according to numerical sequence of the instructions.

There are several parts to the test on each operation code. This is done so that each instruction may be checked under many of the possible ways it can be used. The letter designator associated with each test label has no bearing on what its test is meant to accomplish, except where the r precedes those labels identifying tests containing repeated instructions.

To the right of each instruction word is an explanation of what it is doing or its function in the test. An attempt is made to show the (Q), (A), and the contents of significant addresses as they are changed. All numbers and words are given in octal designation.

TABLE 1. QUAK TEST

PROGRAM: QUAK TEST

DESCRIPTION:
MS - 1 Stop before error type-out.
MS - 2 Stop at the end of QUAK.
MS - 3 Stop after error type-out.
MJ - 3 Repeat QUAK only.

ADDRESS	OP-CODE	u	v	FUNCTION
60000	45	00000	64466	Jump to Start.
60001	56	10000	00002	Stop before error type-out.
60002	22	10000	00017	Store (A_R)
60003	22	00000	00016	Store (A_L)
60004	31	00000	00000	Take y + 1 from f_1, determine
60005	34	00020	00017	address containing print code,
60006	15	32000	00007	and acquire it for (A).
60007	31	00000	00060	Error type-out.
60010	61	00000	32000	Print code in A_0 .... A_5.
60011	34	32000	00006	Delete code that has been used.
60012	47	00010	00013	If (A) is zero, printing is over.
60013	31	00016	00044	Restore (A_L).
60014	32	00017	00000	Restore (A_R).
60015	56	30000	00000	Jump to f_1.
60016	00	00000	00000	= (A_L).
60017	00	00000	00000	= (A_R).
60020	00	00000	00001	Constants
60021	00	00000	00002	
60022	00	00000	00003	
60023	00	00000	00004	
60024	00	00000	00005	
60025	00	00000	00006	
60026	00	00000	00007	
60027	00	00000	00012	
60030	00	00000	00014	
60031	00	00000	00015	
60032	00	00000	00020	
60033	00	00000	00032	
60034	00	00000	00056	
60035	00	00000	00115	
60036	00	00000	00135	
60037	00	00000	00136	
60040	00	00000	00200	
60041	00	00000	00216	
60042	00	00000	00246	
60043	00	00000	00251	

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
60044	00	00000	00254	
60045	00	00000	00256	
60046	00	00000	00266	
60047	00	00000	00314	
60050	00	00000	00321	
60051	00	00000	00327	
60052	00	00000	00344	
60053	00	00000	00355	
60054	00	00000	00377	
60055	00	00000	00505	
60056	00	00000	00522	
60057	00	00000	00777	
60060	00	00000	40000	
60061	00	00001	00000	
60062	00	00032	00000	
60063	00	00117	00000	
60064	00	40000	00000	
60065	00	77777	77777	
60066	01	00000	00000	
60067	04	00000	00003	
60070	05	37373	33135	
60071	07	65432	10000	
60072	10	76543	21000	Constants
60073	14	00000	00000	
60074	20	00000	00000	
60075	23	60000	00000	
60076	30	00000	00004	
60077	30	40506	00000	
60100	30	40506	00045	
60101	30	40506	00073	
60102	32	10321	07654	
60103	32	10765	43210	
60104	32	63242	15243	
60105	35	61414	31313	
60106	37	77777	77241	
60107	37	77777	77713	
60110	37	77777	77730	
60111	37	77777	77742	
60112	37	77777	77744	
60113	37	77777	77745	
60114	37	77777	77746	
60115	37	77777	77750	
60116	37	77777	77762	
60117	40	00000	00000	
60120	40	00000	00032	
60121	40	00000	00035	
60122	40	00000	00064	
60123	40	00000	00536	
60124	42	07601	03710	

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
60125	43	07601	03731	
60126	45	00000	00000	
60127	45	00000	00476	
60130	45	00000	00505	
60131	56	10000	00002	
60132	57	34276	26457	
60133	60	00000	00000	
60134	61	06001	04200	
60135	61	06001	04335	
60136	64	00000	00000	
60137	65	47203	44216	
60140	65	57034	33614	
60141	71	77777	77777	
60142	73	26415	04721	
60143	73	26415	05056	
60144	75	20041	03716	
60145	75	20041	03737	
60146	77	61414	77773	
60147	77	70000	00000	
60150	77	74577	77777	
60151	77	77777	31313	
60152	77	77777	42000	
60153	77	77777	50000	
60154	77	77777	70777	
60155	77	77777	77000	Constants
60156	77	77777	77130	
60157	77	77777	77223	
60160	77	77777	77507	
60161	77	77777	77543	
60162	77	77777	77627	
60163	77	77777	77647	
60164	77	77777	77676	
60165	77	77777	77713	
60166	77	77777	77742	
60167	77	77777	77745	
60170	77	77777	77750	
60171	77	77777	77762	
60172	77	77777	77765	
60173	77	77777	77770	
60174	77	77777	77771	
60175	77	77777	77772	
60176	77	77777	77773	
60177	77	77777	77774	
60200	77	77777	77775	
60201	77	77777	77776	
60202	77	77777	77777	
60203	00	00000	00000	
60204	00	00000	00000	
60205	00	00000	00000	

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION	
60206	00	00000	00000		
60207	00	00000	00000		
60210	11	00203	32000		A = 0
60211	43	32000	00213	11a	Compare (A) = (A), next test
60212	14	52523	00445		failed, Jump to error type-out.
60213	43	00202	00215	43a	Compare -0 with +0 in A failed,
60214	14	64703	00445		Jump to error type-out.
60215	11	00113	32000	11b	A = 37 77777 77745.
60216	43	00120	00236	43b	Compare (A) with (00120).
60217	43	00167	00240	43c	Compare (A) with (00167).
60220	43	00114	00242	43d	Compare (A) with (00114).
60221	43	00112	00244	43e	Compare (A) with (00112).
60222	43	00150	00246	43f	Compare (A) with (00150).
60223	43	00113	00225	11b	Compare (A) with original No.
60224	14	52522	30445		Failed; Jump to error type-out.
60225	11	00167	32000	11c	A = 77 77777 77745.
60226	43	00033	00250	43g	Compare (A) with (00033).
60227	43	00113	00252	43h	Compare (A) with (00113).
60230	43	00114	00254	43i	Compare (A) with (00114).
60231	43	00150	00256	43j	Compare (A) with (00150).
60232	43	00202	00260	43k	Compare (A) with (00202).
60233	43	00167	00235		Compare (A) with original No.
60234	14	52521	60445	11c	Failed; Jump to error type-out;
60235	45	00000	00262		Jump to test 11d.
60236	14	64702	30445	43b	Failed; Jump to error type-out;
60237	45	00000	00217		Jump to test 43c.
60240	14	64701	60445	43c	Failed; Jump to error type-out;
60241	45	00000	00220		Jump to test 43d.
60242	14	64702	20445	43d	Failed; Jump to error type-out;
60243	45	00000	00221		Jump to test 43e.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION	
60244	14	64702	00445	43e	Failed; Jump to error type-out;
60245	45	00000	00222		Jump to test 43f.
60246	14	64702	60445	43f	Failed; Jump to error type-out;
60247	45	00000	00223		Jump to test 11b.
60250	14	64701	30445	43g	Failed; Jump to error type-out;
60251	45	00000	00227		Jump to test 43h.
60252	14	64700	50445	43h	Failed; Jump to error type-out;
60253	45	00000	00230		Jump to test 43i.
60254	14	64701	40445	43i	Failed; Jump to error type-out;
60255	45	00000	00231		Jump to test 43j.
60256	14	64703	20445	43j	Failed; Jump to error type-out;
60257	45	00000	00232		Jump to test 43k.
60260	14	64703	60445	43k	Failed; Jump to error type-out;
60261	45	00000	00233		Jump to test 11c.
60262	11	00202	32000	11d	(A) = 0.
60263	43	00203	00265		Compare (A) with (00203).
60264	14	52522	20445		Failed; Jump to error type-out.
60265	11	00113	32000	11e	(A) = 37 77777 77745.
60266	11	00113	31000		(Q) = 37 77777 77745.
60267	43	31000	00271		Compare (A) with (Q).
60270	14	52522	00445		Failed; Jump to error type-out.
60271	11	31000	00207	11f	(00207) = 37 77777 77745.
60272	43	00207	00274		Compare (A) with (00207).
60273	14	52522	60445		Failed; Jump to error type-out.
60274	11	00114	31000	11g	(Q) = 37 77777 77746.
60275	11	31000	32000		(A) = 37 77777 77746.
60276	43	31000	00300		Compare (A) with (Q);
60277	14	52521	30445		Failed; Jump to error type-out.
60300	43	00114	00302	43L	Compare (A) with original No.
60301	14	64701	10445		Failed; Jump to error type-out.
60302	11	31000	31000	11h	Transmit (Q) to Q.
60303	43	31000	00305		Compare (A) with (Q).
60304	14	52520	50445		Failed; Jump to error type-out.
60305	11	00113	32000	11i	(A) = 37 77777 77745.
60306	43	31000	00345		Compare (A) with (Q).

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION	
60307	11	00167	32000		(A) = 77 77777 77745.
60310	43	31000	00347	11j	Compare (A) with (Q).
60311	11	00165	31000		(Q) = 77 77777 77713.
60312	11	00165	32000		(A) = 77 77777 77713.
60313	43	31000	00315	11k	Compare (A) with (Q).
60314	14	52523	60445		Failed; Jump to error type-out.
60315	11	00113	32000		(A) = 37 77777 77745.
60316	43	31000	00351	11L	Compare (A) with (Q).
60317	11	00120	32000		(A) = 40 00000 00032.
60320	43	31000	00353	11m	Compare (A) with (Q).
60321	11	00104	32000		(A) = 32 63242 15243.
60322	11	00104	00207		(00207) = 32 63242 15243.
60323	43	00207	00325	11n	Compare (A) with (00207)
60324	14	52520	60445		Failed; Jump to error type-out.
60325	11	00103	32000		(A) = 32 10765 43210.
60326	43	00103	00330	11o	Compare (A) with (00103).
60327	14	52520	30445		Failed; Jump to error type-out.
60330	11	00113	32000		(A) = 37 77777 77745.
60331	11	32000	32000		Transmit (A) to A.
60332	43	00113	00334	11p	Compare (A) with (00113)
60333	14	52521	50445		Failed; Jump to error type-out.
60334	11	00106	32000		(A) = 37 77777 77241.
60335	11	32000	00207		(00207) = 37 77777 77241.
60336	43	00207	00340	11q	Compare (A) with (00207)
60337	14	52523	50445		Failed; Jump to error type-out.
60340	11	00105	32000		(A) = 35 61414 31313.
60341	11	32000	31000		(Q) = 35 61414 31313.
60342	43	31000	00344	11r	Compare (A) with (Q).
60343	14	52521	20445		Failed; Jump to error type-out.
60344	45	00000	00355		Jump to test 12a.
60345	14	52521	40445	11i	Failed; Jump to error type-out.
60346	45	00000	00307		Jump to test 11j.
60347	14	52523	20445		Failed; Jump to error type-out.
60350	45	00000	00311	11j	Jump to test 11k.
60351	14	52521	10445		Failed; Jump to error type-out;
60352	45	00000	00317	11L	Jump to test 11m.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
60353	14	52520	70445	11m	Failed; Jump to error type-out;
60354	45	00000	00321		Jump to test 11n.
60355	12	00176	00207		(00207) = +4.
60356	11	00207	32000		(A) = +4.
60357	43	00023	00361	12a	Compare (A) with (00023).
60360	14	52743	00445		Failed; Jump to error type-out.
60361	12	00175	32000		(A) = +5.
60362	43	00024	00364	12b	Compare (A) with (00024).
60363	14	52742	30445		Failed; Jump to error type-out.
60364	12	00177	31000		(Q) = +3.
60365	11	31000	32000		(A) = +3.
60366	43	00022	00370	12c	Compare (A) with (00022).
60367	14	52741	60445		Failed; Jump to error type-out.
60370	11	00025	32000		(A) = +6.
60371	12	32000	00206		(00206) = +6.
60372	11	00206	32000	12d	Transmit (00206) to A.
60373	43	00025	00375		Compare (A) with (00025).
60374	14	52742	20445		Failed; Jump to error type-out.
60375	11	00176	32000		(A) = -4.
60376	12	32000	32000		(A) = +4.
60377	43	00023	00401	12e	Compare (A) with (00023).
60400	14	52742	00445		Failed; Jump to error type-out.
60401	11	00026	32000		(A) = +7.
60402	12	32000	31000		(Q) = +7.
60403	11	31000	32000	12f	Transmit (Q) to A.
60404	43	00026	00406		Compare (A) with (00026).
60405	14	52742	60445		Failed; Jump to error type-out.
60406	11	00176	31000		(Q) = -4.
60407	12	31000	00207		(00207) = +4.
60410	11	00207	32000	12g	(A) = +4.
60411	43	00023	00413		Compare (A) with (00023).
60412	14	52741	30445		Failed; Jump to error type-out.
60413	11	00175	31000		(Q) = -5.
60414	12	31000	32000		(A) = +5.
60415	43	00024	00417	12h	Compare (A) with (00024).
60416	14	52740	50445		Failed; Jump to error type-out.
60417	11	00203	31000		(Q) = 0.
60420	12	31000	31000		Transmit (Q) to Q.
60421	11	31000	32000	12i	(A) = 0.
60422	43	00204	00424		Compare (A) with (00204)

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
60423	14	52741	40445		Failed; Jump to error type-out.
60424	13	00026	00207		(00207) = -7.
60425	11	00207	32000		(A) = -7.
60426	43	00173	00430	13a	Compare (A) with (00173)
60427	14	52703	00445		Failed; Jump to error type-out.
60430	13	00174	32000		(A) = +6.
60431	43	00025	00433	13b	Compare (A) with (00025).
60432	14	52702	30445		Failed; Jump to error type-out.
60433	13	00203	31000		(Q) = all ones.
60434	11	31000	32000		(A) = 0.
60435	43	00203	00437	13c	Compare (A) with (00203)
60436	14	52701	60445		Failed; Jump to error type-out.
60437	11	00024	32000		(A) = +5.
60440	13	32000	00207		(00207) = -5.
60441	11	00207	32000	13d	(A) = -5.
60442	43	00175	00444		Compare (A) with (00175)
60443	14	52702	20445		Failed; Jump to error type-out.
60444	11	00176	32000		(A) = -4.
60445	13	32000	32000		(A) = +4.
60446	43	00023	00450	13e	Compare (A) with (00023).
60447	14	52702	00445		Failed; Jump to error type-out.
60450	11	00022	32000		(A) = +3.
60451	13	32000	31000		(Q) = -3.
60452	11	31000	32000	13f	(A) = -3.
60453	43	00177	00455		Compare (A) with (00177)
60454	14	52702	60445		Failed; Jump to error type-out.
60455	11	00200	31000		(Q) = -2.
60456	13	31000	00207		(00207) = +2.
60457	11	00207	32000	13g	(A) = +2.
60460	43	00021	00462		Compare (A) with (00021).
60461	14	52701	30445		Failed; Jump to error type-out.
60462	11	00203	31000		(Q) = 0.
60463	13	31000	31000		(Q) = all ones.
60464	11	31000	32000	13h	(A) = 0.
60465	43	00203	00467		Compare (A) with (00203).
60466	14	52700	50445		Failed; Jump to error type-out.
60467	11	00176	31000		(Q) = -4.
60470	13	31000	32000		(A) = +4.
60471	43	00023	00473	13i	Compare (A) with (00023)
60472	14	52701	40445		Failed; Jump to error type-out.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
60473	11	00127	00001		Modify F_2.
60474	14	00000	00000		F_1 = MJ to y + 1; Jump to F_2.
60475	45	00000	00475		Constant.
60476	11	00000	32000	14a	(A) = (F_1).
60477	43	00475	00502		Compare (A) with (00475).
60500	11	00131	00001		Restore F_2.
60501	14	52643	00445		Failed; Jump to error type-out.
60502	11	00130	00001		Modify F_2.
60503	14	00000	00000		y + 1 to F_1; Jump to F_2.
60504	45	00000	00504		Constant.
60505	11	00000	32000	14b	(A) = (F_1).
60506	43	00504	00511		Compare (A) with (00504).
60507	11	00131	00001		Restore F_2.
60510	14	52642	30445		Failed; Jump to error type-out.
60511	11	00131	00001		Restore F_2.
60512	11	00176	00207		(00207) = -4.
60513	15	00105	00207		(00207) = 77 61414 77773.
60514	11	00207	32000	15a	(A) = (00207).
60515	43	00146	00517		Compare (A) with (00146).
60516	14	52623	00445		Failed; Jump to error type-out.
60517	11	00176	00207		(00207) = -4.
60520	11	00105	32000		(A) = 35 61414 31313.
60521	15	32000	00207		(00207) = 77 61414 77773.
60522	11	00207	32000	15b	(A) = (00207).
60523	43	00146	00525		Compare (A) with (00146).
60524	14	52622	30445		Failed; Jump to error type-out.
60525	11	00176	00207		(00207) = -4.
60526	11	00105	31000		(Q) = 35 61414 31313.
60527	15	31000	00207		(00207) = 77 61414 77773.
60530	11	00207	32000	15c	(A) = (00207).
60531	43	00146	00533		Compare (A) with (00146).
60532	14	52621	60445		Failed; Jump to error type-out.
60533	11	00176	00207		(00207) = -4.
60534	16	00105	00207		(00207) = 77 77777 31313.
60535	11	00207	32000	16a	(A) = (00207).
60536	43	00151	00540		Compare (A) with (00151).
60537	14	52663	00445		Failed; Jump to error type-out.
60540	11	00176	00207		(00207) = -4.
60541	11	00105	32000		(A) = 35 61414 31313.
60542	16	32000	00207		(00207) = 77 77777 31313.
60543	11	00207	32000	16b	(A) = (00207).
60544	43	00151	00546		Compare (A) with (00207).
60545	14	52662	30445		Failed; Jump to error type-out.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION	
60546	11	00176	00207		(00207) = -4.
60547	11	00105	31000		(Q) = 35 61414 31313.
60550	16	31000	00207	16c	(00207) = 77 77777 31313.
60551	11	00207	32000		(A) = (00207).
60552	43	00151	00554		Compare (A) with (00151).
60553	14	52661	60445		Failed; Jump to error type-out.
60554	11	00065	32000		(A) = 00 77777 77777.
60555	22	10055	00207		(00207) = 7.
60556	11	00207	32000	22a	(A) = 7.
60557	43	00026	00561		Compare (A) with (00026).
60560	14	74743	00445		Failed; Jump to error type-out.
60561	11	00063	32000		(A) = 00 00117 00000.
60562	22	00061	00207		(00207) = 23 60000 00000.
60563	11	00207	32000	22b	(A) = 23 60000 00000.
60564	43	00075	00566		Compare (A) with (00075).
60565	14	74742	30445		Failed; Jump to error type-out.
60566	11	00020	32000		(A) = +1.
60567	22	00045	32000	22c	(A) = +2.
60570	43	00021	00572		Compare (A) with (00021).
60571	14	74741	60445		Failed; Jump to error type-out.
60572	22	00045	32000		(A) = +4.
60573	43	00023	00575	22d	Compare (A) with (00023).
60574	14	74742	20445		Failed; Jump to error type-out.
60575	22	00061	32000		(A) = 00 00001 00000.
60576	43	00061	00600	22e	Compare (A) with (00061).
60577	14	74742	00445		Failed; Jump to error type-out.
60600	22	00062	31000		(Q) = 00 40000 00000.
60601	11	31000	32000	22f	(A) = (Q).
60602	43	00064	00604		Compare (A) with (00064).
60603	14	74742	60445		Failed; Jump to error type-out.
60604	22	10053	31000		(Q) = +1.
60605	11	31000	32000		(A) = +1.
60606	43	00020	00610	22g	Compare (A) with (00020).
60607	14	74741	30445		Failed; Jump to error type-out.
60610	11	00024	00207		(00207) = +5.
60611	21	00207	00021		(00207) = +7.
60612	11	00207	32000	21a	(A) = (00207).
60613	43	00026	00615		Compare (A) with (00026).
60614	14	74523	00445		Failed; Jump to error type-out.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
60615	11	00021	00207		(00207) = +2.
60616	21	00207	32000		(00207) = +4.
60617	11	00207	32000	21b	(A) = (00207).
60620	43	00023	00622		Compare (A) with (00023).
60621	14	74522	30445		Failed; Jump to error type-out.
60622	11	00024	00207		(00207) = +5.
60623	11	00021	31000		(Q) = +2.
60624	21	00207	31000		(00207) = +7.
60625	11	00207	32000	21c	(A) = (00207).
60626	43	00026	00630		Compare (A) with (00026).
60627	14	74521	60445		Failed; Jump to error type-out.
60630	11	00024	32000		(A) = +5.
60631	21	32000	00021		(A) = +7.
60632	43	00026	00634	21d	Compare (A) with (00026)
60633	14	74522	20445		Failed; Jump to error type-out.
60634	11	00021	32000		(A) = +2.
60635	21	32000	32000		(A) = +4.
60636	43	00023	00640	21e	Compare (A) with (00023).
60637	14	74522	00445		Failed; Jump to error type-out.
60640	11	00024	31000		(Q) = +5.
60641	11	00021	32000		(A) = +2.
60642	21	32000	31000	21f	(A) = +7.
60643	43	00026	00645		Compare (A) with (00026).
60644	14	74522	60445		Failed; Jump to error type-out.
60645	11	00024	31000		(Q) = +5.
60646	21	31000	00021		(Q) = +7.
60647	11	31000	32000	21g	(Q) = (A).
60650	43	00026	00652		Compare (A) with (00026).
60651	14	74521	34500		Failed; Jump to error type-out.
60652	11	00021	31000		(Q) = +2.
60653	21	31000	32000		(Q) = +4.
60654	11	31000	32000	21h	(Q) = (A).
60655	43	00023	00657		Compare (A) with (00023).
60656	14	74520	50445		Failed; Jump to error type-out.
60657	11	00021	31000		(Q) = +2.
60660	21	31000	31000		(Q) = +4.
60661	11	31000	32000	21i	(Q) = (A).
60662	43	00023	00664		Compare (A) with (00023).
60663	14	74521	40445		Failed; Jump to error type-out.
60664	11	00026	00207		(00207) = +7.
60665	23	00207	00021	23a	(00207) = +5.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
60666	11	00024	32000		(A) = +5.
60667	43	00207	00671		Compare (A) with (00207).
60670	14	74703	00445		Failed; Jump to error type-out.
60671	11	00105	00207		(00207) = 35 61414 31313.
60672	23	00207	32000		(00207) = 0.
60673	43	00203	00675	23b	Compare (A) with (00203).
60674	14	74702	30445		Failed; Jump to error type-out.
60675	11	00026	00207		(00207) = +7.
60676	11	00024	31000		(Q) = +5.
60677	23	00207	31000		(00207) = +2.
60700	11	00207	32000	23c	(A) = (00207).
60701	43	00021	00703		Compare (A) with (00021).
60702	14	74701	60445		Failed; Jump to error type-out.
60703	11	00026	32000		(A) = +7.
60704	23	32000	00021		(A) = +5.
60705	43	00024	00707	23d	Compare (A) with (00024).
60706	14	74702	20445		Failed; Jump to error type-out.
60707	11	00151	32000		(A) = 77 77777 31313.
60710	23	32000	32000		(A) = 0.
60711	43	00203	00713	23e	Compare (A) with (00203).
60712	14	74702	00445		Failed; Jump to error type-out.
60713	11	00026	32000		(A) = +7.
60714	11	00021	31000		(Q) = +2.
60715	23	32000	31000	23f	(A) = +5.
60716	43	00024	00720		Compare (A) with (00024).
60717	14	74702	60445		Failed; Jump to error type-out.
60720	11	00026	31000		(Q) = +7.
60721	23	31000	00024		(Q) = +2.
60722	11	31000	32000	23g	(Q) = (A).
60723	43	00021	00725		Compare (A) with (00021).
60724	14	74701	30445		Failed; Jump to error type-out.
60725	11	00151	31000		(Q) = 77 77777 31313.
60726	23	31000	32000		(Q) = 0.
60727	11	31000	32000	23h	(Q) = (A).
60730	43	00203	00732		Compare (A) with (00203).
60731	14	74700	50445		Failed; Jump to error type-out.
60732	11	00146	31000		(Q) = 77 61414 77773.
60733	23	31000	31000		(Q) = 0.
60734	11	31000	32000	23i	(Q) = (A).
60735	43	00203	00737		Compare (A) with (00203).
60736	14	74701	40445		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
60737	11	00132	00207		(00207) = 57 34276 26457.
60740	27	00207	00104		(00207) = 65 57034 33614.
60741	11	00207	32000	27a	(A) = (00207).
60742	43	00140	00744		Compare (A) with (00140).
60743	14	74723	00445		Failed; Jump to error type-out.
60744	11	00132	00207		(00207) = 57 34276 26457.
60745	27	00207	32000		(00207) = 0.
60746	11	00207	32000	27b	(A) = (00207).
60747	43	00203	00751		Compare (A) with (00203).
60750	14	74722	30445		Failed; Jump to error type-out.
60751	11	00132	31000		(Q) = 57 34276 26457.
60752	11	00104	00207		(00207) = 32 63242 15243.
60753	27	00207	31000		(00207) = 65 57034 33614.
60754	11	00207	32000	27c	(A) = (00207).
60755	43	00140	00757		Compare (A) with (00140).
60756	14	74721	60445		Failed; Jump to error type-out.
60757	11	00132	32000		(A) = 57 34276 26457.
60760	27	32000	00104		(A) = 65 57034 33614.
60761	43	00140	00763	27d	Compare (A) with (00140).
60762	14	74722	20445		Failed; Jump to error type-out.
60763	11	00116	32000		(A) = 37 77777 77762.
60764	27	32000	32000		(A) = 0.
60765	43	00203	00767	27e	Compare (A) with (00203).
60766	14	74722	00445		Failed; Jump to error type-out.
60767	11	00132	32000		(A) = 57 34276 26457.
60770	11	00104	31000		(Q) = 32 63242 15243.
60771	27	32000	31000	27f	(A) = 65 57034 33614.
60772	43	00140	00774		Compare (A) with (00140).
60773	14	74722	60445		Failed; Jump to error type-out.
60774	11	00132	31000		(Q) = 57 34276 26457.
60775	27	31000	00104		(Q) = 65 57034 33614.
60776	11	31000	32000	27g	(A) = (Q).
60777	43	00140	01001		Compare (A) with (00140).
61000	14	74721	30445		Failed; Jump to error type-out.
61001	27	31000	32000		(Q) = 0.
61002	11	31000	32000		(A) = (Q).
61003	43	00203	01005	27h	Compare (A) with (00203).
61004	14	74720	50445		Failed; Jump to error type-out.
61005	27	31000	31000		(Q) = 0.
61006	11	31000	32000		(A) = (Q).
61007	43	00203	01011	27i	Compare (A) with (00203).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61010	14	74721	40445		Failed; Jump to error type-out.
61011	31	00033	00105		(A_L) = 20 00000 00000.
61012	11	32000	00207		(A_R) = (00207) = +3.
61013	22	00000	32000	31a	(A_R) = 20 00000 00000.
61014	43	00074	01016		Compare (A) with (00074).
61015	14	70523	00445		Failed; Jump to error type-out.
61016	11	00207	32000		(A) = +3.
61017	43	00022	01021	31b	Compare (A) with (00022).
61020	14	70522	30445		Failed; Jump to error type-out.
61021	31	00033	00037		(A_L) = 0.
61022	11	32000	00207		(A_R) = (00207) = 64 00000 00000.
61023	22	00000	32000	31c	(A_R) = 0.
61024	43	00203	01026		Compare (A) with (00203).
61025	14	70521	60445		Failed; Jump to error type-out.
61026	11	00207	32000		(A) = 64 00000 00000.
61027	43	00136	01031	31d	Compare (A) with (00136).
61030	14	70522	20445		Failed; Jump to error type-out.
61031	11	00167	32000		(A) = 62.
61032	31	00114	00044		(A_R) = 77 77777 77777.
61033	11	32000	00207		(00207) = (A_R).
61034	22	00000	32000	31e	(A) = 37 77777 77746.
61035	43	00114	01037		Compare (A) with (00114).
61036	14	70522	00445		Failed; Jump to error type-out.
61037	11	00207	32000		(A) = 0.
61040	43	00203	01042	31f	Compare (A) with (00203).
61041	14	70522	60445		Failed; Jump to error type-out.
61042	31	00113	00000		(A) = 37 77777 77745.
61043	43	00113	01045	31g	Compare (A) with (00113).
61044	14	70521	30445		Failed; Jump to error type-out.
61045	11	00114	32000		(A) = 37 77777 77746.
61046	31	32000	00037		(A_R) = 14 00000 00000.
61047	11	32000	00207		(00207) = (A_R).
61050	31	32000	00002	31h	(A_R) = 60 00000 00000.
61051	11	32000	00206		(00206) = (A_R).
61052	11	00073	32000		(A) = 14 00000 00000.
61053	43	00207	01055		Compare (A) with (00207).
61054	14	70520	50445		Failed; Jump to error type-out.
61055	11	00133	32000		(A) = 60 00000 00000.
61056	43	00206	01060	31i	Compare (A) with (00206).
61057	14	70521	40445		Failed; Jump to error type-out.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61060	31	00167	00064		(A_R) = 00 00001 77777.
61061	31	32000	00044		(A_R) = 0.
61062	11	32000	00207		(A_R) = (00207).
61063	11	00203	32000	31j	(A) = 0.
61064	43	00207	01066		Compare (A) with (00207)
61065	14	70523	20445		Failed; Jump to error type-out.
61066	11	00120	32000		(A_R) = 40 00000 00032.
61067	31	32000	00017		(A_R) = 00 00032 00000.
61070	11	32000	00207	31k	(31a-) (A_R) = (00207).
61071	22	00000	32000		(A_R) = 00 00000 40000.
61072	43	00060	01074		Compare (A) with (00060).
61073	14	70523	60445		Failed; Jump to error type-out.
61074	11	00207	32000		(A) = 00 00032 00000.
61075	43	00062	01077	31L	Compare (A) with (00062).
61076	14	70521	10445		Failed; Jump to error type-out.
61077	31	00120	00017		(A_R) = 00 00032 00000.
61100	11	32000	00207		(A_R) = (00207).
61101	11	00062	32000	31m	(31a-) (A_R) = 00 00032 00000.
61102	43	00207	01104		Compare (A) with (00207).
61103	14	70520	70445		Failed; Jump to error type-out.
61104	31	00120	00105		(A_R) = 04 00000 00003.
61105	11	32000	00207		(A_R) = (00207).
61106	22	00000	32000	31n	(A_R) = 20 00000 00000.
61107	43	00074	01111		Compare (A) with (00074).
61110	14	70520	60445		Failed; Jump to error type-out.
61111	11	00207	32000		(A) = 04 00000 00003.
61112	43	00067	01114	31o	Compare (A) with (00067).
61113	14	70520	30445		Failed; Jump to error type-out.
61114	11	00033	31000		(Q) = 00 00000 00032.
61115	31	31000	00105		(A_R) = 00 00000 00003.
61116	11	32000	00207		(A_R) = (00207).
61117	22	00000	32000	31p	(A_R) = 20 00000 00000.
61120	43	00074	01122		Compare (A) with (00074).
61121	14	70521	50445		Failed; Jump to error type-out.
61122	11	00207	32000		(A) = +3.
61123	43	00022	01125	31q	Compare (A) with (00022).
61124	14	70523	50445		Failed; Jump to error type-out.
61125	11	00033	31000		(Q) = +32.
61126	31	31000	00037		(A_R) = 64 00000 00000.
61127	11	32000	00207	31r	(00207) = (A_R).
61130	22	00000	32000		(A_R) = 0.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61131	43	00203	01133		Compare (A) with (00203).
61132	14	70521	20445		Failed; Jump to error type-out.
61133	11	00207	32000		(A) = 64 00000 00000.
61134	43	00136	01136	31s	Compare (A) with (00136).
61135	14	70522	40445		Failed; Jump to error type-out.
61136	11	00167	31000		(Q) = -32.
61137	31	31000	00036		(A_R) = 45 00000 00000.
61140	11	32000	00207		(00207) = (A_R).
61141	22	00000	32000	31t	(A_R) = 00 77777 77777.
61142	43	00065	01144		Compare (A) with (00065).
61143	14	70520	10445		Failed; Jump to error type-out.
61144	11	00207	32000		(A) = 45 00000 00000.
61145	43	00126	01147	31u	Compare (A) with (00126).
61146	14	70523	40445		Failed; Jump to error type-out.
61147	11	00167	31000		(Q) = -32.
61150	31	31000	00102		(A_R) = 00 77777 77777.
61151	11	32000	00207		(00207) = (A_R).
61152	22	00000	32000	31v	(A_R) = 45 00000 00000.
61153	43	00126	01155		Compare (A) with (00126).
61154	14	70521	70445		Failed; Jump to error type-out.
61155	11	00207	32000		(A) = 00 77777 77777.
61156	43	00065	01160	31w	Compare (A) with (00065).
61157	14	70523	10445		Failed; Jump to error type-out.
61160	11	00113	32000		(A) = 37 77777 77745.
61161	32	00022	00011		(A_R) = 77 77777 50000.
61162	11	32000	00207		(00207) = (A_R).
61163	22	00000	32000	32a	(A_R) = 00 00000 00377.
61164	43	00054	01166		Compare (A) with (00054).
61165	14	70743	00445		Failed; Jump to error type-out.
61166	11	00207	32000		(A) = 77 77777 50000.
61167	43	00153	01171	32b	Compare (A) with (00153).
61170	14	70742	30445		Failed; Jump to error type-out.
61171	11	00167	32000		(A_R) = 77 77777 77745.
61172	32	00167	00000		(A_R) = 77 77777 77713.
61173	11	32000	00207		(00207) = (A_R).
61174	22	00000	32000	32c	(A) = 0.
61175	43	00203	01177		Compare (A) with (00203).
61176	14	70741	60445		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61177	11	00207	32000		(A) = 77 77777 77713.
61200	43	00165	01202	32d	Compare (A) with (00165).
61201	14	70742	20445		Failed; Jump to error type-out.
61202	11	00203	32000		(A) = 0.
61203	32	00202	00003		(A_L) = 00 00000 00007.
61204	32	00203	00006		(A_L) = 00 00000 00777.
61205	11	32000	00207	32e	(00207) = 77 77777 77000.
61206	22	00000	32000		(A_R) = 00 00000 00777.
61207	43	00057	01211		Compare (A) with (00057).
61210	14	70742	00445		Failed; Jump to error type-out.
61211	11	00207	32000		(A) = 77 77777 77000.
61212	43	00155	01214	32f	Compare (A) with (00155).
61213	14	70742	60445		Failed; Jump to error type-out.
61214	11	00167	32000		(A_R) = 77 77777 77745.
61215	32	32000	00003		(A_R) = 77 77777 77130.
61216	11	32000	00207		(00207) = 77 77777 77130.
61217	22	00000	32000	32g	(A_R) = 00 00000 00007.
61220	43	00026	01222		Compare (A) with (00026).
61221	14	70741	34500		Failed; Jump to error type-out.
61222	11	00207	32000		(A) = 77 77777 77130.
61223	43	00156	00225	32h	Compare (A) with (00156).
61224	14	70740	50445		Failed; Jump to error type-out.
61225	11	00033	32000		(A) = +32.
61226	32	32000	00036		(A) = 64 00000 00000.
61227	22	10000	32000	32i	(A) = 64 00000 00000.
61230	43	00136	01232		Compare (A) with (00136).
61231	14	70741	40445		Failed; Jump to error type-out.
61232	11	00167	32000		(A) = -32.
61233	11	00167	31000		(Q) = -32.
61234	32	31000	00003		(A_L) = 00 00000 00007.
61235	11	32000	00207	32j	(00207) = 77 77777 77130.
61236	22	00000	32000		(A) = 00 00000 00007.
61237	43	00026	01241		Compare (A) with (00026).
61240	14	70743	20445		Failed; Jump to error type-out.
61241	11	00207	32000		(A) = 77 77777 77130.
61242	43	00156	01244	32k	Compare (A) with (00156).
61243	14	70743	60445		Failed; Jump to error type-out.
61244	11	00067	32000		(A) = 04 00000 00003.
61245	11	00067	31000		(Q) = (A).
61246	32	31000	00041	32L	(A_L) = 01 00000 00000.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61247	11	32000	00207		(00207) = 60 00000 00000.
61250	22	00000	32000		(A_R) = 01 00000 00000.
61251	43	00066	01253		Compare (A) with (00066).
61252	14	70741	10445		Failed; Jump to error type-out.
61253	11	00207	32000		(A) = 60 00000 00000.
61254	43	00133	01256	32m	Compare (A) with (00133).
61255	14	70740	70445		Failed; Jump to error type-out.
61256	33	00202	00003		(A_L) = 77 77777 77770.
61257	11	32000	00207		(00207) = 00 00000 00007.
61260	22	00000	32000	33a	(A_R) = 77 77777 77770.
61261	43	00173	01263		Compare (A) with (00173).
61262	14	70703	00445		Failed; Jump to error type-out.
61263	11	00207	32000		(A) = +7.
61264	43	00026	01266	33b	Compare (A) with (00026).
61265	14	70702	30445		Failed; Jump to error type-out.
61266	33	00167	00047		(A_L) = 00 00000 00327.
61267	11	32000	00207		(00207) = 77 77777 77770.
61270	22	00000	32000	33c	(A_R) = 00 00000 00327.
61271	43	00051	01273		Compare (A) with (00051).
61272	14	70701	60445		Failed; Jump to error type-out.
61273	11	00207	32000		(A) = 77 77777 77770.
61274	43	00173	01276	33d	Compare (A) with (00173).
61275	14	70702	20445		Failed; Jump to error type-out.
61276	33	00033	00000		(A) = 77 77777 77745.
61277	43	00167	01301	33e	Compare (A) with (00167).
61300	14	70702	00445		Failed; Jump to error type-out.
61301	11	00033	32000		(A) = +32.
61302	33	32000	00025		(A_R) = 77 74577 77777.
61303	11	32000	00207		(00207) = (A_R).
61304	22	00000	32000	33f	(A_R) = 77 77777 77777.
61305	43	00203	01307		Compare (A) with (00203).
61306	14	70702	60445		Failed; Jump to error type-out.
61307	11	00207	32000		(A) = 77 74577 77777.
61310	43	00150	01312	33g	Compare (A) with (00150).
61311	14	70701	30445		Failed; Jump to error type-out.
61312	11	00173	32000		(A) = -7.
61313	33	32000	00033		(A_R) = 00 77777 77777.
61314	11	32000	00207	33h	(00207) = (A_R).
61315	22	00000	32000		(A_R) = 77 70000 00000.
61316	43	00147	01320		Compare (A) with (00147).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61317	14	70700	50445		Failed; Jump to error type-out.
61320	11	00207	32000		(A) = 00 77777 77777.
61321	43	00065	01323	33i	Compare (A) with (00065).
61322	14	70701	40445		Failed; Jump to error type-out.
61323	11	00033	31000		(Q) = +32.
61324	33	31000	00025		(A_R) = 77 74577 77777.
61325	11	32000	00207		(00207) = (A_R).
61326	22	00000	32000	33j	(A_R) = 0.
61327	43	00203	01331		Compare (A) with (00203).
61330	14	70703	20445		Failed; Jump to error type-out.
61331	11	00207	32000		(A) = 77 74577 77777.
61332	43	00150	01334	33k	Compare (A) with (00150).
61333	14	70703	60445		Failed; Jump to error type-out.
61334	11	00113	32000		(A) = 37 77777 77745.
61335	34	00022	00011		(A_R) = 77 77777 42000.
61336	11	32000	00207		(00207) = (A_R).
61337	22	00000	32000	34a	(A_R) = 00 00000 00377.
61340	43	00054	01342		Compare (A) with (00054).
61341	14	70643	00445		Failed; Jump to error type-out.
61342	11	00207	32000		(A) = 77 77777 42000.
61343	43	00152	01345	34b	Compare (A) with (00152).
61344	14	70642	30445		Failed; Jump to error type-out.
61345	11	00022	32000		(A) = +3.
61346	34	00120	00003		(A_R) = 77 77777 77507.
61347	11	32000	00207		(00207) = (A_R).
61350	22	00000	32000	34c	(A_R) = 77 77777 77773.
61351	43	00176	01353		Compare (A) with (00176).
61352	14	70641	60445		Failed; Jump to error type-out.
61353	11	00207	32000		(A) = 77 77777 77507.
61354	43	00160	01356	34d	Compare (A) with (00160).
61355	14	70642	20445		Failed; Jump to error type-out.
61356	11	00167	32000		(A) = -32.
61357	34	32000	00003		(A_R) = 00 00000 00007.
61360	11	32000	00207		(00207) = (A_R).
61361	22	00000	32000	34e	(A_R) = 77 77777 77770,
61362	43	00173	01364		Compare (A) with (00173).
61363	14	70642	00445		Failed; Jump to error type-out.
61364	11	00207	32000		(A) = 7.
61365	43	00026	01367	34f	Compare (A) with (00026).
61366	14	70642	60445		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61367	11	00022	32000		(A) = +3.
61370	34	32000	00006		(A) = 0.
61371	43	00203	01373	34g	Compare (A) with (00203).
61372	14	70641	30445		Failed; Jump to error type-out.
61373	11	00033	32000		(A) = 32.
61374	11	00022	31000		(Q) = 3.
61375	34	31000	00001	34h	(A) = 56.
61376	43	00034	01400		Compare (A) with (00034).
61377	14	70640	50445		Failed; Jump to error type-out.
61400	11	00203	32000		(A) = 0.
61401	11	00133	31000		(Q) = 60 00000 00000.
61402	34	31000	00105	34i	(A_R) = 71 77777 77777.
61403	43	00141	01405		Compare (A) with (00141).
61404	14	70641	40445		Failed; Jump to error routine.
61405	11	00022	32000		(A) = +3.
61406	35	00113	00207		(00207) = 37 77777 77750.
61407	43	00207	01411	35a	Compare (A) with (00207).
61410	14	70623	00445		Failed; Jump to error type-out.
61411	11	00115	32000		(A) = 37 77777 77750.
61412	43	00207	01414	35b	Compare (A) with (00207).
61413	14	70622	30445		Failed; Jump to error type-out.
61414	11	00022	32000		(A) = +3.
61415	35	00171	00207		(00207) = 77 77777 77765.
61416	11	00172	32000	35c	(A) = 77 77777 77765.
61417	43	00207	01421		Compare (A) with (00207).
61420	14	70621	60445		Failed; Jump to error type-out.
61421	11	00120	32000		(A) = 40 00000 00032.
61422	35	00167	00207		(00207) = 40 00000 00000.
61423	11	00117	32000	35d	(A) = 40 00000 00000.
61424	43	00207	01426		Compare (A) with (00207).
61425	14	70622	20445		Failed; Jump to error type-out.
61426	11	00167	32000		(A) = -32.
61427	35	00022	00207		(00207) = -27.
61430	43	00170	01432	35e	Compare (A) with (00170).
61431	14	70622	00445		Failed; Jump to error type-out.
61432	11	00113	32000		(A) = 37 77777 77745.
61433	35	00022	32000		(A) = 37 77777 77750.
61434	43	00115	01436	35f	Compare (A) with (00115).
61435	14	70622	60445		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61436	11	00031	32000		(A) = +15.
61437	35	00177	32000		(A) = +12.
61440	43	00027	01442	35g	Compare (A) with (00027).
61441	14	70621	30445		Failed; Jump to error type-out.
61442	11	00167	32000		(A) = -32.
61443	35	00120	31000		(Q) = 40 00000 00000.
61444	11	00117	32000	35h	(A) = 40 00000 00000.
61445	43	31000	01447		Compare (A) with (Q).
61446	14	70620	50445		Failed; Jump to error type-out.
61447	11	00177	32000		(A) = -3.
61450	35	00031	31000		(Q) = +12.
61451	11	00027	32000	35i	(A) = +12.
61452	43	31000	01454		Compare (A) with (Q).
61453	14	70621	40445		Failed; Jump to error type-out.
61454	11	00171	32000		(A) = -15.
61455	35	32000	00207		(00207) = -32.
61456	11	00207	32000	35j	(A) = -32.
61457	43	00167	01461		Compare (A) with (00167).
61460	14	70623	20445		Failed; Jump to error type-out.
61461	11	00031	32000		(A) = +15.
61462	35	32000	32000		(A) = +32.
61463	43	00033	01465	35k	Compare (A) with (00033).
61464	14	70623	60445		Failed; Jump to error type-out.
61465	11	00171	32000		(A) = -15.
61466	35	32000	31000		(Q) = -32.
61467	11	00167	32000	35L	(A) = -32.
61470	43	31000	01472		Compare (A) with (Q).
61471	14	70621	10445		Failed; Jump to error type-out.
61472	11	00113	32000		(A) = 37 77777 77745.
61473	11	00171	31000		(Q) = -15.
61474	35	31000	00207		(00207) = 37 77777 77730.
61475	11	00110	32000	35m	(A) = 37 77777 77730.
61476	43	00207	01500		Compare (A) with (00207).
61477	14	70620	70445		Failed; Jump to error type-out.
61500	11	00033	32000		(A) = +32.
61501	11	00171	31000		(Q) = -15.
61502	35	31000	32000	35n	(A) = +15.
61503	43	00031	01505		Compare (A) with (00031).
61504	14	70620	60445		Failed; Jump to error type-out.
61505	11	00113	32000		(A) = 37 77777 77745.
61506	11	00022	31000	35o	(Q) = +3.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61507	35	31000	31000		(Q) = 37 77777 77750.
61510	11	00115	32000		(A) = 37 77777 77750.
61511	43	31000	01513		Compare (A) with (Q).
61512	14	70620	30445		Failed; Jump to error type-out.
61513	11	00022	32000		(A) = +3.
61514	36	00113	00207		(00207) = 40 00000 00035.
61515	43	00207	01517	36a	Compare (A) with (00207).
61516	14	70663	00445		Failed; Jump to error type-out.
61517	11	00121	32000		(A) = 40 00000 00035.
61520	43	00207	01522	36b	Compare (A) with (00207).
61521	14	70662	30445		Failed; Jump to error type-out.
61522	11	00022	32000		(A) = +3.
61523	36	00171	00207		(00207) = +20.
61524	11	00032	32000	36c	(A) = +20.
61525	43	00207	01527		Compare (A) with (00207).
61526	14	70661	60445		Failed; Jump to error type-out.
61527	11	00120	32000		(A) = 40 00000 00032.
61530	36	00167	00207		(00207) = 40 00000 00064.
61531	11	00122	32000	36d	(A) = 40 00000 00064.
61532	43	00207	01534		Compare (A) with (00207).
61533	14	70662	20445		Failed; Jump to error type-out.
61534	11	00167	32000		(A) = -32.
61535	36	00022	00207		(00207) = -35.
61536	11	00166	32000	36e	(A) = -35.
61537	43	00207	01541		Compare (A) with (00207).
61540	14	70662	00445		Failed; Jump to error type-out.
61541	11	00113	32000		(A) = 37 77777 77745.
61542	36	00022	32000		(A) = 37 77777 77742.
61543	43	00111	01545	36f	Compare (A) with (00111).
61544	14	70662	60445		Failed; Jump to error type-out.
61545	11	00167	32000		(A) = -32.
61546	11	00120	31000		(Q) = 40 00000 00032.
61547	36	31000	31000		(Q) = 37 77777 77713.
61550	11	00107	32000	36g	(A) = 37 77777 77713.
61551	43	31000	01553		Compare (A) with (Q).
61552	14	70661	30445		Failed; Jump to error type-out.
61553	36	32000	00207		(00207) = 0.
61554	11	00203	32000		(A) = 0.
61555	43	00207	01557	36h	Compare (A) with (00207).
61556	14	70660	50445		Failed; jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61557	11	00113	32000		(A) = 37 77777 77745.
61560	36	32000	32000		(A) = 0.
61561	43	00203	01563	36i	Compare (A) with (00203).
61562	14	70661	40445		Failed; Jump to error type-out.
61563	11	00150	32000		(A) = 77 74577 77777.
61564	36	32000	31000		(A) = (Q) = 0.
61565	43	00203	01567	36j	Compare (A) with (00203).
61566	14	70663	20445		Failed; Jump to error type-out.
61567	11	00113	32000		(A) = 37 77777 77745.
61570	11	00171	31000		(Q) = -15.
61571	36	31000	00207		(00207) = 37 77777 77762.
61572	11	00116	32000	36k	(A) = 37 77777 77762.
61573	43	00207	01575		Compare (A) with (00207).
61574	14	70663	60445		Failed; Jump to error type-out.
61575	11	00120	32000		(A) = 40 00000 00032.
61576	11	00167	31000		(Q) = -32.
61577	36	31000	32000	36L	(A) = 40 00000 00064.
61600	43	00122	01602		Compare (A) with (00122).
61601	14	70661	10445		Failed; Jump to error type-out.
61602	11	00022	32000		(A) = +3.
61603	11	00113	31000		(Q) = 37 77777 77745.
61604	36	31000	31000		(Q) = 40 00000 00035.
61605	11	00121	32000	36m	(A) = 40 00000 00035.
61606	43	31000	01610		Compare (A) with (Q).
61607	14	70660	70445		Failed; Jump to error type-out.
61610	11	00024	00207		(00207) = +5.
61611	41	00207	01613	41a	(A) = +4 (positive).
61612	14	64523	04500		Failed; Jump to error type-out.
61613	41	00207	01615		(A) = +3 (positive).
61614	14	64522	34500	41b	Failed; Jump to error type-out.
61615	41	00207	01617		(A) = +2 (positive).
61616	14	64521	64500	41c	Failed; Jump to error type-out.
61617	41	00207	01621		(A) = +1 (positive).
61620	14	64522	24500	41d	Failed; Jump to error type-out.
61621	41	00207	01623		(A) = 0 (positive).
61622	14	64522	04500	41e	Failed; Jump to error type-out.
61623	41	00207	01660	41f	(A) = -1 (negative).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61624	11	00203	32000		(A) = 0.
61625	43	00207	01627	41g	Compare (A) with (00207).
61626	14	64521	34500		Failed; Jump to error type-out.
61627	37	00207	01631		(00207) = 00 00000 01630.
61630	00	00000	01630		Constant.
61631	11	00207	32000	37a	(A) = (00207).
61632	43	01630	01634		Compare (A) with (01630).
61633	14	70723	04500		Failed; Jump to error type-out.
61634	37	00207	01636		(00207) = 00 00000 01635.
61635	00	00000	01635		Constant.
61636	11	00207	32000	37b	(A) = 00 00000 01635.
61637	43	01635	01641		Compare (A) with (01635).
61640	14	70722	34500		Failed; Jump to error type-out.
61641	11	00021	32000		(A) = +2.
61642	41	32000	01644	41h	(A) = +1 (positive).
61643	14	64520	54500		Failed; Jump to error type-out.
61644	41	32000	01646		(A) = 0 (positive).
61645	14	64521	44500	41i	Failed; Jump to error type-out.
61646	41	32000	01662	41j	(A) = -1 (negative).
61647	43	00201	01651		Compare (A) with (00201).
61650	14	64523	64500	41k	Failed; Jump to error type-out.
61651	11	00020	31000		(Q) = +1.
61652	41	31000	01654	41L	(A) = 0 (positive).
61653	14	64521	14500		Failed; Jump to error type-out.
61654	41	31000	01665	41m	(A) = -1 (negative).
61655	11	00203	32000		(A) = 0.
61656	43	31000	01667	41n	Compare (A) with (Q).
61657	45	00000	01666		Jump to 01666.
61660	14	64522	64500		Failed; Jump to error type-out.
61661	45	00000	01624	41f	Jump to test 41g.
61662	14	64523	24500		Failed; Jump to error type-out.
61663	45	00000	01647	41j	Jump to test 41k.
61664	14	64520	74500		Failed; Jump to error type-out.
61665	45	00000	01655	41m	Jump to test 41n.
61666	14	64520	64500		Failed; Jump to error type-out.
61667	11	00067	32000	41n	(A) = 04 00000 00003.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION	
61670	42	00113	01672		(A) is negative.
61671	14	64743	04500	42a	Failed; Jump to error type-out.
61672	11	00114	32000		(A) = 37 77777 77746.
61673	42	00113	01721	42b	(A) is positive.
61674	43	00114	01676		Compare (A) with (00114).
61675	14	64741	64500	42c	Failed; Jump to error type-out.
61676	11	00150	32000		(A) = 77 74577 77777.
61677	42	00153	01701	42d	(A) is negative.
61700	14	64742	24500		Failed; Jump to error type-out.
61701	11	00150	32000		(A) = 77 74577 77777.
61702	42	00136	01723	42e	(A) is positive.
61703	11	00033	32000		(A) = +32.
61704	42	00167	01725	42f	(A) is positive.
61705	11	00167	32000		A = -32.
61706	42	00113	01710	42g	A is negative.
61707	14	64741	34500		Failed; Jump to error type-out.
61710	11	00122	32000		(A) = 40 00000 00064.
61711	42	32000	01727	42h	(A) = 0 (positive).
61712	11	00033	31000		(Q) = +32.
61713	42	31000	01715	42i	(A) = -32 (negative).
61714	14	64741	44500		Failed; Jump to error type-out.
61715	11	00113	32000		(A) = 37 77777 77745.
61716	11	00033	31000		(Q) = +32.
61717	42	31000	01731	42j	A is positive.
61720	45	00000	01732		Jump to test 44a.
61721	14	64742	34500		Failed; Jump to error type-out.
61722	45	00000	01674	42b	Jump to test 42c.
61723	14	64742	04500		Failed; Jump to error type-out.
61724	45	00000	01703	42e	Jump to test 42f.
61725	14	64742	64500		Failed; Jump to error type-out.
61726	45	00000	01705	42f	Jump to test 42g.
61727	14	64740	54500		Failed; Jump to error type-out.
61730	45	00000	01712	42h	Jump to test 42i.
61731	14	64743	24500	42j	Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
61732	11	00020	31000		(Q) = +1.
61733	44	01734	01735	44a	Q is positive, Jump to test 44b.
61734	14	64643	04500		Failed; Jump to error type-out.
61735	11	31000	32000		(A) = +2.
61736	43	00021	01740	44b	Compare (A) with (00021).
61737	14	64642	34500		Failed; Jump to error type-out.
61740	11	00167	31000		(Q) = -32.
61741	44	01743	01742	44c	Q is negative, Jump to test 44d.
61742	14	64641	64500		Failed; Jump to error type-out.
61743	11	31000	32000		(A) = -64.
61744	43	00165	01746	44d	Compare (A) with (00165).
61745	14	64642	24500		Failed; Jump to error type-out.
61746	11	00117	32000		(A) = 40 00000 00000.
61747	46	01751	01750	46a	A is negative, Jump to test 46b.
61750	14	64663	04500		Failed; Jump to error type-out.
61751	11	00112	32000		(A) = 37 77777 77742.
61752	46	01753	01754	46b	A is positive, Jump to test 47a.
61753	14	64662	34500		Failed; Jump to error type-out.
61754	11	00022	32000		(A) = +3.
61755	47	01757	01756	47a	A is no zero, Jump to test 47b.
61756	14	64723	04500		Failed; Jump to error type-out.
61757	43	00022	01761		Compare (A) with (00022).
61760	14	64722	34500	47b	Failed; Jump to error type-out.
61761	11	00203	32000		(A) =0.
61762	47	01763	01764	47c	A is zero, Jump to test 51a.
61763	14	64721	64500		Failed; Jump to error type-out.
61764	11	00142	31000		(Q) = 73 26415 04721.
61765	51	00137	00207		(00207) = 61 06001 04200.
61766	11	00134	32000	51a	(A) = 61 06001 04200.
61767	43	00207	01771		Compare (A) with (00207).
61770	14	62523	00445		Failed; Jump to error type-out.
61771	51	00137	32000		(A) = 61 06001 04200.
61772	27	32000	00134		(A) = 0.
61773	43	00203	01775	51b	Compare (A) with (00203).
61774	14	62522	30445		Failed; Jump to error type-out.
61775	51	00137	31000		(Q) = 61 06001 04200.
61776	11	31000	32000	51c	(A) = (Q).
61777	43	00134	02001		Compare (A) with (00134).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62000	14	62521	60445		Failed; Jump to error type-out.
62001	11	00142	31000		(Q) = 73 26415 04721.
62002	11	00137	32000		(A) = 65 47203 44216.
62003	51	32000	00207		(00207) = 61 06001 04200.
62004	11	00207	32000	51d	(A) = (00207).
62005	43	00134	02007		Compare (A) with (00207).
62006	14	62522	20445		Failed; Jump to error type-out.
62007	11	00137	32000		(A) = 65 47203 44216.
62010	51	32000	32000		(A) = 61 06001 04200.
62011	27	32000	00134	51e	(A) = 0.
62012	43	00203	02014		Compare (A) with (00203).
62013	14	62522	00445		Failed; Jump to error type-out.
62014	11	00137	32000		(A) = 65 47203 44216.
62015	51	32000	31000		(Q) = 61 06001 04200.
62016	11	31000	32000	51f	(A) = 61 06001 04200.
62017	43	00134	02021		Compare (A) with (00134).
62020	14	62522	60445		Failed; Jump to error type-out.
62021	11	00142	31000		(Q) = 73 26415 04721.
62022	51	31000	00207		(00207) = (Q).
62023	11	00207	32000	51g	(A) = (00207).
62024	43	00142	02026		Compare (A) with (00142).
62025	14	62521	30445		Failed; Jump to error type-out.
62026	51	31000	32000		(A) = 73 26415 04721.
62027	27	32000	00142		(A) = 0.
62030	43	00203	02032	51h	Compare (A) with (00203).
62031	14	62520	50445		Failed; Jump to error type-out.
62032	51	31000	31000		(Q) = 73 26415 04721.
62033	11	31000	32000		(A) = (Q).
62034	43	00142	02036	51i	Compare (A) with (00142).
62035	14	62521	40445		Failed; Jump to error type-out.
62036	11	00036	32000		(A) = +135.
62037	11	00142	31000		(Q) = 73 26415 04721.
62040	52	00137	00207		(00207) = 61 06001 04335.
62041	11	00207	32000	52a	(A) = (00207).
62042	43	00135	02044		Compare (A) with (00135).
62043	14	62743	00445		Failed; Jump to error type-out.
62044	11	00036	32000		(A) = +135.
62045	52	00137	32000		(A) = 61 06001 04335.
62046	27	32000	00135	52b	(A) = 0.
62047	43	00203	02051		Compare (A) with (00203).
62050	14	62742	30445		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62051	11	00036	32000		(A) = +135.
62052	52	00137	31000		(Q) = 61 06001 04335.
62053	11	31000	32000	52c	(A) = (Q).
62054	43	00135	02056		Compare (A) with (00135).
62055	14	62741	60445		Failed; Jump to error type-out.
62056	11	00036	32000		(A) = +135.
62057	11	00142	31000		(Q) = 73 26415 04721.
62060	52	32000	00207		(00207) = 00 00000 256.
62061	11	00207	32000	52d	(A) = (00207).
62062	43	00045	02064		Compare (A) with (00045).
62063	14	62742	20445		Failed; Jump to error type-out.
62064	11	00036	32000		(A) = +135.
62065	52	32000	32000		(A) = +256.
62066	43	00045	02070	52e	Compare (A) with (00045).
62067	14	62742	00445		Failed; Jump to error type-out.
62070	11	00036	32000		(A) = +135.
62071	52	32000	31000		(Q) = +256.
62072	11	31000	32000	52f	(A) = (Q).
62073	43	00045	02075		Compare (A) with (00045).
62074	14	62742	60445		Failed; Jump to error type-out.
62075	11	00142	31000		(Q) = 73 26415 04721.
62076	11	00036	32000		(A) = +135.
62077	52	31000	00207		(00207) = 73 26415 05056.
62100	11	00207	32000	52g	(A) = (00207).
62101	43	00143	02103		Compare (A) with (00143).
62102	14	62741	30445		Failed; Jump to error type-out.
62103	11	00142	31000		(Q) = 73 26415 04721.
62104	11	00036	32000		(A) = +135.
62105	52	31000	32000		(A) = 73 26415 05056.
62106	27	32000	00143	52h	(A) = 0.
62107	43	00203	02111		Compare (A) with (00203).
62110	14	62740	50445		Failed; Jump to error type-out.
62111	11	00142	31000		(Q) = 73 26415 04721.
62112	11	00036	32000		(A) = +135.
62113	52	31000	31000		(Q) = 73 26415 05056.
62114	11	31000	32000	52i	(A) = (Q).
62115	43	00143	02117		Compare (A) with (00143).
62116	14	62741	40445		Failed; Jump to error type-out.
62117	11	00035	31000		(Q) = +115.
62120	11	00052	00207		(00207) = 00 00000 00344.
62121	53	00041	00207	53a	(00207) = 00 00000 00254.
62122	11	00207	32000		(A) = (00207).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62123	43	00044	02125		Compare (A) with (00044).
62124	14	62703	00445		Failed; Jump to error type-out.
62125	11	00052	32000		(A) = +344.
62126	53	00041	32000		(A) = +14.
62127	43	00030	02131	53b	Compare (A) with (00030).
62130	14	62702	30445		Failed; Jump to error type-out.
62131	53	00041	31000		(Q) = 77 77777 77676.
62132	27	31000	00164		(Q) = 0.
62133	11	31000	32000	53c	(A) = 0.
62134	43	00203	02136		Compare (A) with (00203).
62135	14	62701	60445		Failed; Jump to error type-out.
62136	11	00041	32000		(A) = +216.
62137	11	00035	31000		(Q) = +115.
62140	11	00052	00207		(00207) = +344.
62141	53	32000	00207	53d	(00207) = +254.
62142	11	00207	32000		(A) = (00207).
62143	43	00044	02145		Compare (A) with (00044).
62144	14	62702	20445		Failed; Jump to error type-out.
62145	11	00041	32000		(A) = +216.
62146	53	32000	32000		(A) = +14.
62147	43	00030	02151	53e	Compare (A) with (00030).
62150	14	62702	00445		Failed; Jump to error type-out.
62151	11	00041	32000		(A) = +216.
62152	53	32000	31000		(Q) = 77 77777 77676.
62153	11	31000	32000	53f	(A) = (Q).
62154	43	00164	02156		Compare (A) with (00164).
62155	14	62702	60445		Failed; Jump to error type-out.
62156	11	00035	31000		(Q) = +115.
62157	11	00052	00207		(00207) = +344.
62160	53	31000	00207		(00207) = +355.
62161	11	00207	32000	53g	(A) = (00207).
62162	43	00053	02164		Compare (A) with (00053).
62163	14	62701	30445		Failed; Jump to error type-out.
62164	11	00052	32000		(A) = +344.
62165	53	31000	32000		(A) = +115.
62166	43	00035	02170	53h	Compare (A) with (00035).
62167	14	62700	50445		Failed; Jump to error type-out.
62170	53	31000	31000		(Q) = 77 77777 77777.
62171	11	31000	32000		(A) = 0.
62172	43	00203	02174	53i	Compare (A) with (00203).
62173	14	62701	40445		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62174	11	00103	00207		(00207) = 32 10765 43210.
62175	54	00207	00011		(A_R) = 07 65432 10000.
62176	54	32000	00044		(A_R) = 00 00000 00321.
62177	22	10000	32000	54a	(A_R) = 00 00000 00321.
62200	43	00050	02202		Compare (A) with (00050).
62201	14	62643	00445		Failed; Jump to error type-out.
62202	11	00207	32000		(A_R) = 07 65432 10000.
62203	43	00071	02205	54b	Compare (A) with (00071).
62204	14	62642	30445		Failed; Jump to error type-out.
62205	11	00103	31000		(Q) = 32 10765 43210.
62206	54	31000	00055		(Q) = 00 00000 00321.
62207	54	32000	00044		(A_R) = 07 65432 10000.
62210	22	10000	32000	54c	(A_R) = 07 65432 10000.
62211	43	00071	02213		Compare (A) with (00071).
62212	14	62641	60445		Failed; Jump to error type-out.
62213	11	31000	32000		(A) = 00 00000 00321.
62214	43	00050	02216	54d	Compare (A) with (00050).
62215	14	62642	20445		Failed; Jump to error type-out.
62216	11	00103	32000		(A) = 32 10765 43210.
62217	54	32000	00006		(A_R) = 10 76543 21000.
62220	11	32000	00207		(00207) = (A_R).
62221	54	32000	00044	54e	(A_R) = 00 00000 00032.
62222	22	10000	32000		(A_R) = 00 00000 00032.
62223	43	00033	02225		Compare (A) with (00033).
62224	14	62642	00445		Failed; Jump to error type-out.
62225	11	00207	32000		(A) = 10 76543 21000.
62226	43	00072	02230	54f	Compare (A) with (00072).
62227	14	62642	60445		Failed; Jump to error type-out.
62230	11	00167	31000		(Q) = -32.
62231	55	31000	00025		(Q) = 77 74577 77777.
62232	11	31000	32000	55a	(A) = (Q).
62233	43	00150	02235		Compare (A) with (00150).
62234	14	62623	00445		Failed; Jump to error type-out.
62235	11	00103	00207		(00207) = 32 10765 43210.
62236	55	00207	00044		(00207) = 32 10765 43210.
62237	11	00207	32000	55b	(A) = (00207).
62240	43	00103	02242		Compare (A) with (00103).
62241	14	62622	30445		Failed; Jump to error type-out.
62242	11	00103	00207		(00207) = 32 10765 43210.
62243	55	00207	00030	55c	(00207) = 32 10321 07654.
62244	11	00207	32000		(A) = (00207).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62245	43	00102	02247		Compare (A) with (00102).
62246	14	62621	60445		Failed; Jump to error type-out.
62247	11	00173	32000		(A) = -7.
62250	55	32000	00011		(A) = 77 77777 70777.
62251	43	00154	02253	55d	Compare (A) with (00154).
62252	14	62622	20445		Failed; Jump to error type-out.
62253	71	00113	00171		(A_R) = 40 00000 00536.
62254	11	32000	00207		(00207) = (A_R).
62255	22	00000	32000	71a	(A_R) = 77 77777 77771.
62256	43	00174	02260		Compare (A) with (00174).
62257	14	72523	00445		Failed; Jump to error type-out.
62260	11	00207	32000		(A) = 40 00000 00536.
62261	43	00123	02263	71b	Compare (A) with (00123).
62262	14	72522	30445		Failed; Jump to error type-out.
62263	71	00171	00113		(A_R) = 40 00000 00536.
62264	11	32000	00207		(00207) = (A_R).
62265	22	00000	32000	71c	(A_R) = 77 77777 77771.
62266	43	00174	02270		Compare (A) with (00174).
62267	14	72521	60445		Failed; Jump to error type-out.
62270	11	00207	32000		(A) = 40 00000 00536.
62271	43	00123	02273	71d	Compare (A) with (00123).
62272	14	72522	20445		Failed; Jump to error type-out.
62273	71	00171	00120		(A_R) = 37 77777 77241.
62274	11	32000	00207		(00207) = (A_R).
62275	22	00000	32000	71e	(A_R) = 00 00000 00006.
62276	43	00025	02300		Compare (A) with (00025).
62277	14	72522	00445		Failed; Jump to error type-out.
62300	11	00207	32000		(A) = 37 77777 77241.
62301	43	00106	02303	71f	Compare (A) with (00106).
62302	14	72522	60445		Failed; Jump to error type-out.
62303	71	00113	00031		(A_R) = 37 77777 77241.
62304	11	32000	00207		(00207) = (A_R).
62305	22	00000	32000	71g	(A_R) = 00 00000 00006.
62306	43	00025	02310		Compare (A) with (00025).
62307	14	72521	30445		Failed; Jump to error type-out.
62310	11	00207	32000		(A) = 37 77777 77241.
62311	43	00106	02313	71h	Compare (A) with (00106).
62312	14	72520	50445		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62313	71	00202	00113		(A) = 0.
62314	43	00203	02316	71i	Compare (A) with (00203).
62315	14	72521	40445		Failed; Jump to error type-out.
62316	71	00113	00202		(A) = 0.
62317	43	00203	02321	71j	Compare (A) with (00203).
62320	14	72523	20445		Failed; Jump to error type-out.
62321	11	00113	32000		A = 37 77777 77745.
62322	71	00113	32000		(A) = 0.
62323	43	00203	02325	71k	Compare (A) with (00203).
62324	14	72523	60445		Failed; Jump to error type-out.
62325	11	00113	31000		(Q) = 37 77777 77745.
62326	71	00171	31000		(A_R) = 00 00000 00251.
62327	43	00043	02331	71L	Compare (A) with (00043).
62330	14	72521	10445		Failed; Jump to error type-out.
62331	11	00113	31000		(Q) = 37 77777 77745.
62332	71	00031	31000		(A) = 00 00000 00251.
62333	43	00043	02335	71m	Compare (A) with (00043).
62334	14	72520	70445		Failed; Jump to error type-out.
62335	11	00031	32000		(A) = +15.
62336	71	32000	00033		(A) = +522.
62337	43	00056	02341	71n	Compare (A) with (00056).
62340	14	72520	60445		Failed; Jump to error type-out.
62341	11	00120	32000		(A) = 40 00000 00032.
62342	71	32000	00171		(A_R) = 37 77777 77241.
62343	11	32000	00207		(00207) = (A_R).
62344	22	00000	32000	71o	(A_R) = 00 00000 00006.
62345	43	00025	02347		Compare (A) with (00025).
62346	14	72520	30445		Failed; Jump to error type-out.
62347	11	00207	32000		(A) = 37 77777 77241.
62350	43	00106	02352	71p	Compare (A) with (00106).
62351	14	72521	50445		Failed; Jump to error type-out.
62352	11	00022	32000		(A) = +3.
62353	71	32000	32000		(A) = 0.
62354	43	00203	02356	71q	Compare (A) with (00203).
62355	14	72523	50445		Failed; Jump to error type-out.
62356	11	00171	32000		(A) = 77 77777 77762.
62357	11	00103	31000		(Q) = 32 10765 43210.
62360	71	32000	31000	71r	(A_R) = 00 00000 00251.
62361	11	32000	00207		(00207) = (A_R).
62362	22	00000	32000		(A_R) = 0.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62363	43	00203	02365		Compare (A) with (00203).
62364	14	72521	20445		
62365	11	00207	32000		(A) = 00 00000 00251.
62366	43	00043	02370	71s	Compare (A) with (00043).
62367	14	72522	40445		Failed; Jump to error type-out.
62370	11	00031	32000		(A) = +15.
62371	11	00113	31000		(Q) = 37 77777 77745.
62372	71	32000	31000		(A_R) = 00 00000 00251.
62373	11	32000	00207	71t	(00207) = (A_R).
62374	22	00000	32000		(A_R) = 0.
62375	43	00203	02377		Compare (A) with (00203).
62376	14	72520	10445		Failed; Jump to error type-out.
62377	11	00207	32000		(A) = 00 00000 00251.
62400	43	00043	02402	71u	Compare (A) with (00043).
62401	14	72523	40445		Failed; Jump to error type-out.
62402	11	00031	31000		(Q) = +15.
62403	71	31000	00113		(A_R) = 37 77777 77241.
62404	11	32000	00207		(00207) = (A_R).
62405	22	00000	32000	71v	(A_R) = 00 00000 00006.
62406	43	00025	02410		Compare (A) with (00025).
62407	14	72521	70445		Failed; Jump to error type-out.
62410	11	00207	32000		(A) = 37 77777 77241.
62411	43	00106	02413	71w	Compare (A) with (00106).
62412	14	72523	10445		Failed; Jump to error type-out.
62413	11	00171	31000		(Q) = -15.
62414	71	31000	00120		(A_R) = 37 77777 77241.
62415	11	32000	00207		(00207) = (A_R).
62416	22	00000	32000	71x	(A_R) = 00 00000 00006.
62417	43	00025	02421		Compare (A) with (00025).
62420	14	72522	70445		Failed; Jump to error type-out.
62421	11	00207	32000		(A) = 37 77777 77241.
62422	43	00106	02424	71y	Compare (A) with (00106).
62423	14	72522	50445		Failed; Jump to error type-out.
62424	11	00120	31000		(Q) = 40 00000 00032.
62425	71	31000	00031		(A_R) = 40 00000 00536.
62426	11	32000	00207		(00207) = (A_R).
62427	22	00000	32000	71z	(A_R) = 77 77777 77771.
62430	43	00174	02432		Compare (A) with (00174).
62431	14	72522	10450		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION	
62432	11	00207	32000		(A) = 40 00000 00536.
62433	43	00123	02435	71aa	Compare (A) with (00123).
62434	14	72523	03045		Failed; Jump to error type-out.
62435	11	00113	32000		(A) = 37 77777 77745.
62436	11	00113	31000		(Q) = 37 77777 77745.
62437	71	31000	32000	71bb	(A) = 0.
62440	43	00203	02442		Compare (A) with (00203).
62441	14	72522	32345		Failed; Jump to error type-out.
62442	11	00031	31000		(Q) = +15.
62443	71	31000	31000		(A) = +251.
62444	43	00043	02446	71cc	Compare (A) with (00043).
62445	14	72521	61645		Failed; Jump to error type-out.
62446	11	00171	31000		(Q) = -15.
62447	71	31000	31000		(A) = +251.
62450	43	00043	02452	71dd	Compare (A) with (00043).
62451	14	72522	22245		Failed; Jump to error type-out.
62452	11	00022	32000		(A) = +3.
62453	72	00171	00026		(A) = 77 77777 77647.
62454	43	00163	02456	72a	Compare (A) with (00163).
62455	14	72743	00445		Failed; Jump to error type-out.
62456	11	00022	32000		(A) = +3.
62457	72	00031	00026		(A) = +136.
62460	43	00037	02462	72b	Compare (A) with (00037).
62461	14	72742	30445		Failed; Jump to error type-out.
62462	11	00171	32000		(A) = -15.
62463	72	00026	00171		(A) = 77 77777 77627.
62464	43	00162	02466	72c	Compare (A) with (00162).
62465	14	72741	60445		Failed; Jump to error type-out.
62466	11	00171	32000		(A) = -15.
62467	72	00171	00167		(A) = 00 00000 00505.
62470	43	00055	02472	72d	Compare (A) with (00055).
62471	14	72742	20445		Failed; Jump to error type-out.
62472	11	00113	32000		(A) = 37 77777 77745.
62473	72	00113	32000		(A_R) = 37 77777 77745.
62474	43	00113	02476	72e	Compare (A) with (00113).
62475	14	72742	00445		Failed; Jump to error type-out.
62476	11	00177	32000		(A) = -3.
62477	11	00113	31000		(Q) = 37 77777 77745.
62500	72	00031	31000	72f	(A) = 00 00000 00246.
62501	43	00042	02503		Compare (A) with (00042).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62502	14	72742	60445		Failed; Jump to error type-out.
62503	11	00022	32000		(A) = +3.
62504	11	00167	31000		(Q) = 77 77777 77745.
62505	72	00171	31000	72g	(A) = 00 00000 00254.
62506	43	00044	02510		Compare (A) with (00044).
62507	14	72741	30445		Failed; Jump to error type-out.
62510	11	00167	32000		(A) = -32.
62511	72	32000	00031		(A) = 77 77777 77223.
62512	43	00157	02514	72h	Compare (A) with (00157).
62513	14	72740	50445		Failed; Jump to error type-out.
62514	11	00031	32000		(A) = +15.
62515	72	32000	00171		(A) = 77 77777 77543.
62516	43	00161	02520	72i	Compare (A) with (00161).
62517	14	72741	40445		Failed; Jump to error type-out.
62520	11	00076	32000		(A) = 30 00000 00004.
62521	54	32000	00003		(A_R) = 00 00000 00040.
62522	72	32000	32000		(A_R) = 00 00000 00200.
62523	11	32000	00207	72j	(00207) = (A_R).
62524	22	00000	32000		(A_R) = 00 00000 00003.
62525	43	00022	02527		Compare (A) with (00022).
62526	14	72743	20445		Failed; Jump to error type-out.
62527	11	00207	32000		(A) = 00 00000 00200.
62530	43	00040	02532	72k	Compare (A) with (00040).
62531	14	72743	60445		Failed; Jump to error type-out.
62532	11	00031	32000		(A) = +15.
62533	72	32000	31000		(A) = +266.
62534	43	00046	02536	72L	Compare (A) with (00046).
62535	14	72741	10445		Failed; Jump to error type-out.
62536	11	00171	32000		(A) = -15.
62537	11	00171	31000		(Q) = -15.
62540	72	31000	00026	72m	(A) = -150.
62541	43	00162	02543		Compare (A) with (00162).
62542	14	72740	70445		Failed; Jump to error type-out.
62543	31	00067	00006		(A_R) = 00 00000 00300.
62544	11	00022	31000		(Q) = +3.
62545	72	31000	32000		(A_R) = 00 00000 00314.
62546	11	32000	00207	72n	(00207) = (A_R).
62547	22	00000	32000		(A_R) = 00 00000 00005.
62550	43	00023	02552		Compare (A) with (00023).
62551	14	72740	60445		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
62552	11	00207	32000	(A) = +314.
62553	43	00047	02555	72o Compare (A) with (00047)
62554	14	72740	30445	Failed; Jump to error type-out.
62555	11	00022	32000	(A) = +3.
62556	11	00031	31000	(Q) = +15.
62557	72	31000	31000	72p (A) = +254.
62560	43	00044	02562	Compare (A) with (00044).
62561	14	72741	50445	Failed; Jump to error type-out.
62562	11	00024	32000	(A) = +5.
62563	73	00022	00207	(A) = +2.
62564	43	00021	02566	73a Compare (A) with (00021).
62565	14	72703	00445	Failed; Jump to error type-out.
62566	11	00207	32000	(A) = +1.
62567	43	00020	02571	73b Compare (A) with (00020).
62570	14	72702	34500	Failed; Jump to error type-out.
62571	11	00175	32000	(A) = -5.
62572	73	00177	00207	(A) = +1.
62573	43	00020	02575	73c Compare (A) with (00020).
62574	14	72701	64500	Failed; Jump to error type-out.
62575	11	00207	32000	(A) = +2.
62576	43	00021	02600	73d Compare (A) with (00021).
62577	14	72702	24500	Failed; Jump to error type-out.
62600	11	00024	32000	(A) = +5.
62601	73	00177	00207	(A) = +2.
62602	43	00021	02604	73e Compare (A) with (00021).
62603	14	72702	04500	Failed; Jump to error type-out.
62604	11	00207	32000	(A) = -1.
62605	43	00201	02607	73f Compare (A) with (00201).
62606	14	72702	64500	Failed; Jump to error type-out.
62607	11	00175	32000	(A) = -5.
62610	73	00022	00207	(A) = +1.
62611	43	00020	02613	73g Compare (A) with (00020).
62612	14	72701	34500	Failed; Jump to error type-out.
62613	11	00207	32000	(A) = -2.
62614	43	00200	02616	73h Compare (A) with (00200).
62615	14	72700	54500	Failed; Jump to error type-out.
62616	11	00024	32000	(A) = +5.
62617	73	00177	32000	73i (A) = -1.
62620	43	00201	02622	Compare (A) with (00201).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62621	14	72701	44500		Failed; Jump to error type-out.
62622	11	00175	32000		(A) = -5.
62623	73	00177	31000		(Q) = +2, (A) = +1.
62624	43	00020	02626	73j	Compare (A) with (00020).
62625	14	72703	44500		Failed; Jump to error type-out.
62626	11	31000	32000		(A) = +2.
62627	43	00021	02631	73k	Compare (A) with (00021).
62630	14	72703	64500		Failed; Jump to error type-out.
62631	11	00175	32000		(A) = -5.
62632	73	32000	00207		(A) = 0.
62633	43	00203	02635	73L	Compare (A) with (00203).
62634	14	72701	14500		Failed; Jump to error type-out.
62635	11	00207	32000		(A) = +1.
62636	43	00020	02640	73m	Compare (A) with (00020).
62637	14	72700	74500		Failed; Jump to error type-out.
62640	11	00142	32000		(A) 73 26415 04721.
62641	73	32000	32000	73n	(A) = +1.
62642	43	00020	02644		Compare (A) with (00020).
62643	14	72700	64500		Failed; Jump to error type-out.
62644	11	00137	32000		(A) = 65 47203 44216.
62645	73	32000	31000		(A) = 0, (Q) = +1.
62646	43	00203	02650	73o	Compare (A) with (00203).
62647	14	72700	34500		Failed; Jump to error type-out.
62650	11	31000	32000		(A) = +1.
62651	43	00020	02653	73p	Compare (A) with (00020).
62652	14	72701	54500		Failed; Jump to error type-out.
62653	11	00177	31000		(Q) = -3.
62654	11	00024	32000		(A) = +5.
62655	73	31000	00207	73q	(A) = +2.
62656	43	00021	02660		Compare (A) with (00021).
62657	14	72703	54500		Failed; Jump to error type-out.
62660	11	00207	32000		(A) = -1.
62661	43	00201	02663	73r	Compare (A) with (00201).
62662	14	72701	24500		Failed; Jump to error type-out.
62663	11	00175	32000		(A) = -5.
62664	11	00022	31000		(Q) = +3.
62665	73	31000	32000	73s	(A) = -2.
62666	43	00200	02670		Compare (A) with (00200).
62667	14	72702	44500		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
62670	11	00175	32000	(A) = -5.
62671	11	00177	31000	(Q) = -3.
62672	73	31000	31000	73t (A) = +1, (Q) = +2.
62673	43	00020	02675	Compare (A) with (00020).
62674	14	72700	14500	Failed; Jump to error type-out.
62675	11	31000	32000	(A) = +2.
62676	43	00021	02700	73u Compare (A) with (00021).
62677	14	72703	44500	Failed; Jump to error type-out.
62700	11	00077	00207	(00207) = 30 40506 00000.
62701	74	00063	00207	(A) = 23 60000 00000.
62702	43	00075	02704	74a Compare (A) with (00075).
62703	14	72643	04500	Failed; Jump to error type-out.
62704	11	00207	32000	(A) = 30 40506 00073.
62705	43	00101	02707	74b Compare (A) with (00101).
62706	14	72642	34500	Failed; Jump to error type-out.
62707	74	00203	00207	(A) = 0.
62710	11	00207	32000	(A) = 30 40506 00045.
62711	43	00100	02713	74c Compare (A) with (00100).
62712	14	72641	64500	Failed; Jump to error type-out.
62713	11	00063	32000	(A) = 00 00117 00000.
62714	74	32000	00207	(A) = 23 60000 00000.
62715	43	00075	02717	74d Compare (A) with (00075).
62716	14	72642	24500	Failed; Jump to error type-out.
62717	11	00207	32000	(A) = 30 40506 00073.
62720	43	00101	02722	74e Compare (A) with (00101).
62721	14	72642	04500	Failed; Jump to error type-out.
62722	11	00063	31000	(Q) = 00 00117 00000.
62723	74	31000	00207	(A) = 23 60000 00000.
62724	43	00075	02726	74f Compare (A) with (00075).
62725	14	72642	64500	Failed; Jump to error type-out.
62726	11	00207	32000	(A) = 30 40506 00073.
62727	43	00101	02731	74g Compare (A) with (00101).
62730	14	72641	34500	Failed; Jump to error type-out.
62731	75	00000	02734	"n" = 0, no repeat, jump to test 75b.
62732	45	00000	02733	75a Jump to failure entry
62733	14	72523	04500	Failed; Jump to error type-out.
62734	75	07777	02736	Repeat, n = 7777.
62735	45	00000	02737	75b Jump to test 75c, end repeat.
62736	14	72522	34500	Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
62737	11	00020	31000		(Q) = +1.
62740	11	31000	32000		(A) = +1.
62741	75	75034	02741		First repeat (is not performed).
62742	75	00037	02745		Second repeat, repeats (02744).
62743	35	31000	31000	75c	Not used, leads to failure.
62744	35	31000	32000		(A) = +40.
62745	54	32000	00103		(A) = +1.
62746	43	00020	02750		Compare (A) with (00020).
62747	14	72521	64500		Failed; Jump to error type-out.
62750	45	00000	02751		Jump to floating point test. (not used yet).
62751	11	00065	07601		(07601) = 00 77777 77777.
62752	75	30176	02754		Repeat, n = 176.
62753	11	07601	07602		(07601) = (07776).
62754	11	07776	32000	r11a	(A) = 00 77777 77777.
62755	43	07601	02757		Compare (A) with (07601).
62756	14	12525	23045		Failed; Jump to error type-out.
62757	11	00102	32000		(A) = 32 10321 07654.
62760	75	10176	02762		Transfer (A) to (07776).
62761	11	32000	07601		
62762	23	07776	07601	r11b	(A) = 0.
62763	47	02764	02765		Check (A) for zero.
62764	14	12525	22345		Failed; Jump to error type-out.
62765	11	00061	31000		(Q) = 00 00001 00000.
62766	75	10176	02770		Transfer (Q) to (07776).
62767	11	31000	07601		
62770	23	07776	07601	r11c	(A) = 0.
62771	47	02772	02773		Check (A) for zero.
62772	14	12525	21645		Failed; Jump to error type-out.
62773	75	10177	02775		Transfer (00173) to (07601) thru
62774	11	00173	07601		to (07777).
62775	75	30175	02777		Change (07601) thru (07775)
62776	12	07602	07601	r12a	from -7 to +7.
62777	21	07601	07776		Add (07601) to (07776), A = 0.
63000	47	03001	03002		Check (A) for zero.
63001	14	12527	43045		Failed; Jump to error type-out.
63002	11	00175	32000		(A) = -5.
63003	75	10176	03005		Transfer +5 to (07601)
63004	12	32000	07601		thru (07776).
63005	75	20176	03007		Add -5 to (07601) thru
63006	21	07601	00175	r12b	(07776).
63007	75	10176	03011		Add (07601) thru (07776).
63010	21	32000	07601		(A) = 0.
63011	47	03012	03013		Check (A) for zero.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
63012	14	12527	42345	Failed; Jump to error type-out.
63013	11	00173	31000	(Q) = -7.
63014	75	10176	03016	} Transfer +7 to (07601)
63015	12	31000	07601	} thru (07776).
63016	75	20176	03020	} Add -7 to (07601)
63017	21	07601	31000	r12c } thru (07776).
63020	75	30176	03022	} Add (07601) thru (07776).
63021	35	07601	07601	} (A) = 0.
63022	47	03023	03024	Check (A) is zero.
63023	14	12527	41645	Failed; Jump to error type-out.
63024	11	00026	07601	(07601) = +7.
63025	75	30175	03027	} Transmit -7 to (07602)
63026	13	07601	07602	} thru (07777).
63027	21	07601	07776	r13a Add (07601) to (07776), A = 0.
63030	47	03031	03032	Check (A) is zero.
63031	14	12527	03045	Failed; Jump to error type-out.
63032	11	00057	32000	(A) = +777.
63033	75	10176	03035	} Transmit -777 to (07601)
63034	13	32000	07601	} thru (07776).
63035	21	32000	07776	Add (A) to (07776), A = 0.
63036	21	32000	00057	r13b Add (A) to (00057), A = +777.
63037	21	32000	07601	Add (A) to (07601), A = 0.
63040	47	03041	03042	Check (A) is zero.
63041	14	12527	02345	Failed; Jump to error type-out.
63042	11	00026	31000	(Q) = +7.
63043	75	10176	03045	} Transmit -7 to (07601) thru
63044	13	31000	07601	} (07776).
63045	75	20175	03047	r13c } Add +7 to (07601) thru (07776).
63046	21	07601	31000	
63047	47	03050	03051	Check (A) is zero.
63050	14	12527	01645	Failed; Jump to error type-out.
63051	75	10177	03053	} Transmit -4 to (07601)
63052	11	00176	07601	} thru (07777).
63053	15	00105	07601	(07601) = 77 61414 77773.
63054	75	30175	03056	} Transmit "u" of (07601) to
63055	15	07601	07602	r15a } (07602) thru (07777).
63056	11	07776	32000	(A) = 77 61414 77773.
63057	43	07601	03061	Compare (A) with (07601).
63060	14	12526	23045	Failed; Jump to error type-out.
63061	75	10177	03063	} Transmit (00063) to (07601)
63062	11	00063	07601	} thru (07777).
63063	11	00203	32000	r15b (A) = 0.
63064	75	10177	03066	

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
63065	15	32000	07601		Transmit "u" of (A) to (07601) thru (07777).
63066	43	07601	03070		Compare (A) with (07601).
63067	14	12526	22345		Failed; Jump to error type-out.
63070	43	07700	03072		Compare (A) with (07700).
63071	14	12526	21645	r15c	Failed; Jump to error type-out.
63072	43	07776	03074		Compare (A) with (07776).
63073	14	12526	22245	r15d	Failed; Jump to error type-out.
63074	75	10177	03076		Transmit -4 to (07601)
63075	11	00176	07601		thru (07777).
63076	11	00146	31000		(Q) = 77 61414 77773.
63077	75	10177	03101		Transmit "u" of Q to
63100	15	31000	07601	r15e	(07601) thru (07777).
63101	11	31000	32000		(A) = 77 61414 77773.
63102	43	07601	03104		Compare (A) with (07601).
63103	14	12526	22045		Failed; Jump to error type-out.
63104	43	07700	03106		Compare (A) with (07700).
63105	14	12526	22645	r15f	Failed; Jump to error type-out.
63106	43	07776	03110		Compare (A) with (07776).
63107	14	12526	21345	r15g	Failed; Jump to error type-out.
63110	75	10177	03112		Transmit all ones to
63111	11	00202	07601		(07601) thru (07777).
63112	16	00105	07601		(07601) = 77 77777 31313.
63113	75	30176	03115		Transmit (07601) to (07602)
63114	16	07601	07602	r16a	thru (07777).
63115	23	07601	07776		(A) = 0.
63116	47	03117	03120		Check (A) for zero.
63117	14	12526	63045		Failed; Jump to error type-out.
63120	75	10177	03122		Transmit (00127) to
63121	11	00127	07601		(07601) thru (07777).
63122	11	00130	32000		(A) = 45 00000 00505.
63123	75	10177	03125	r16b	Transmit "v" of (A) to
63124	16	32000	07601		(07601) thru (07777).
63125	43	07601	03127		Compare (A) with (07601).
63126	14	12526	62345		Failed; Jump to error type-out.
63127	43	07700	03131		Compare (A) with (07700).
63130	14	12526	61645	r16c	Failed; Jump to error type-out.
63131	43	07776	03133		Compare (A) with (07776).
63132	14	12526	62245	r16d	Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
63133	75	10177	03135	} Transmit all ones to
63134	11	00202	07601	} (07601) thru (07777).
63135	11	00153	31000	(Q) = 77 77777 50000.
63136	75	10177	03140	r16e } Transmit "v" of (Q) to
63137	16	31000	07601	} (07601) thru (07777).
63140	11	31000	32000	(A) = (Q).
63141	43	07601	03143	Compare (A) with (07601).
63142	14	12526	62045	Failed; Jump to error type-out.
63143	43	07700	03145	Compare (A) with (07700).
63144	14	12526	62645	r16f Failed; Jump to error type-out.
63145	43	07776	03147	Compare (A) with (07776).
63146	14	12526	61345	r16g Failed; Jump to error type-out.
63147	75	10177	03151	} Transmit all zeros to
63150	11	00203	07601	} (07601) thru (07777).
63151	11	00057	32000	(A) = 00 00000 00777.
63152	75	10177	03154	r22a } Transmit (A_R) to (07601)
63153	22	10110	07601	} thru (07777).
63154	43	07601	03156	Compare (A) with (07601).
63155	14	12747	43045	Failed; Jump to error type-out.
63156	43	07700	03160	Compare (A) with (07700).
63157	14	12747	42345	r22b Failed; Jump to error type-out.
63160	43	07776	03162	Compare (A) with (07776).
63161	14	12747	41645	r22c Failed; Jump to error type-out.
63162	31	00055	00044	(A_R) = 0, (A_L) = 00 00000 00505.
63163	75	10177	03165	} Transmit (A_L) to (07601)
63164	22	00110	07601	} thru (07777).
63165	54	32000	00044	r22d Shift A, A_R = 00 00000 00505.
63166	43	07601	03170	Compare (A) with (07601).
63167	14	12747	42245	Failed; Jump to error type-out.
63170	43	07700	03172	Compare (A) with (07700).
63171	14	12747	42045	r22e Failed; Jump to error type-out.
63172	43	07776	03174	Compare (A) with (07776).
63173	14	12747	42645	r22f Failed; Jump to error type-out.
63174	11	00065	32000	(A) = 00 77777 77777.
63175	75	00777	03177	} Shift A 72 places 777
63176	22	10110	32000	r22g } times.
63177	43	00065	03201	Compare (A) with (00065).
63200	14	12747	41345	Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
63201	11	00020	32000		(A) = +1.
63202	75	00573	03204		} Repeatedly transmit (A_L)
63203	22	00177	31000		} to (Q), shifting (A) each time.
63204	11	31000	32000	r22h	(A) = (Q) = +2.
63205	43	00021	03207		Compare (A) with (00021).
63206	14	12747	40545		Failed; Jump to error type-out.
63207	11	00203	32000		(A) = 0.
63210	11	00024	07601		(07601) = +5.
63211	75	30175	03213		} Odd addresses between 07601 &
63212	13	07601	07602		} 07776 = +5; even addresses = -5.
63213	75	10176	03215	r21a	} Alternately add +5 and -5
63214	21	32000	07601		} to (A).
63215	47	03216	03217		Check (A) for zero.
63216	14	12745	23045		Failed; Jump to error type-out.
63217	27	31000	31000		(Q) = 0.
63220	75	10176	03222		} Alternately add +5 and -5
63221	21	31000	07601	r21b	} to (Q).
63222	47	03223	03224		Check A for zero.
63223	14	12745	22345		Failed; Jump to error type-out.
63224	75	30175	03226		}
63225	21	07601	07602		} (07601) thru (07775) = 0.
63226	75	10175	03230		} Add (07601) thru (07775)
63227	21	32000	07601	r21c	} to (A). (A) = 0.
63230	43	07775	03232		Compare (A) with (07775).
63231	14	12745	21645		Failed; Jump to error type-out.
63232	11	00026	31000		Q = +7.
63233	75	10177	03235		} Addresses (07601) thru
63234	11	00026	07601		} (07777) = +7.
63235	55	31000	00007		Shift (Q) to equal +1600.
63236	13	31000	32000	r21d	(A) = -1600.
63237	75	10177	03241		} Add +7 to (A) 177 times
63240	21	32000	07601		
63241	43	00173	03243		Compare (A) with (00173).
63242	14	12745	22245		Failed; Jump to error type-out.
63243	11	00024	00207		Set (00207) to +5.
63244	55	00207	00011		Shift (00207) to +5000.
63245	11	00203	32000		(A) = 0.
63246	11	00024	31000		(Q) = +5.
63247	75	01000	03251	r21e	}
63250	21	32000	31000		} Add (Q) to (A) 1000 times.
63251	43	00207	03253		Compare (A) with (00207).
63252	14	12745	22045		Failed; Jump to error type-out.
63253	11	00020	31000	r21f	Q = +1.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
63254	75	00045	03256	r21f	Add (Q) to (Q) 45 times
63255	21	31000	31000		exceeding modulus.
63256	43	00021	03260		Compare (A) with (00021).
63257	14	12745	22645		Failed; Jump to error type-out.
63260	75	10176	03262		(07601) thru (07776) = +7.
63261	11	00026	07601		
63262	11	00203	31000		(Q) = 0.
63263	75	10176	03265		Add +7 to (Q) 176 times.
63264	21	31000	07601		
63265	75	20176	03267	r21g	Add +1562 to (07601)
63266	21	07601	32000		thru (07776).
63267	75	10175	03271		Sum (07601) thru (07776)
63270	21	32000	07601		in (A).
63271	23	32000	31000		(A) - (Q) to (A).
63272	43	31000	03274		Compare (A) with (Q).
63273	14	12745	21345		Failed; Jump to error type-out.
63274	11	00020	32000		(A) = +1.
63275	75	00045	03277	r21h	Add (A) to (A) 45 times
63276	21	32000	32000		exceeding modulus.
63277	43	00021	03301		Compare (A) with (00021).
63300	14	12745	20545		Failed; Jump to error type-out.
63301	11	00020	31000		(Q) = +1.
63302	75	00044	03304		Add (Q) to (Q) 44 times
63303	21	31000	32000		exceeding modulus.
63304	11	31000	32000	r21i	(Q) = (A) = +1.
63305	43	00020	03307		Compare (A) with (00020).
63306	14	12745	21445		Failed; Jump to error type-out.
63307	75	10176	03311		(07601) thru (07776) = +5.
63310	11	00024	07601		
63311	75	30175	03313		(07601) thru (07775) = 0
63312	23	07601	07602		(07776) = +5.
63313	75	10176	03315	r23a	(A) + (07601) thru (07776).
63314	21	32000	07601		
63315	43	00024	03317		Compare (A) with (00024).
63316	14	12747	03045		Failed; Jump to error type-out.
63317	11	00173	31000		(Q) = -7.
63320	75	20175	03322		(07601) thru (07775) = +7.
63321	23	07601	31000		
63322	75	10100	03324		Sum (07601) thru (07700)
63323	21	32000	07601	r23b	in A. (A) = +707.
63324	55	31000	00006		Shift (Q) to -700.
63325	21	32000	31000		Add (Q) to (A).
63326	43	00026	03330		Compare (A) with (00026).
63327	14	12747	02345		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
63330	75	10176	03332		
63331	11	00175	07601		(07601) thru (07776) = -5.
63332	11	00203	32000		(A) = 0.
63333	75	10100	03335		Subtract -5 from A 100 times.
63334	23	32000	07601	r23c	(A) = +500.
63335	22	00036	32000		(A) = +5.
63336	43	00024	03340		Compare (A) with (00024).
63337	14	12747	01645		Failed; Jump to error type-out.
63340	13	00154	32000		(A) = +7000.
63341	11	00026	31000		(Q) = +7.
63342	75	01000	03344		Subtract (Q) from (A)
63343	23	32000	31000	r23d	1000 times.
63344	47	03345	03346		Check (A) = 0.
63345	14	12747	02245		Failed; Jump to error type-out.
63346	11	00203	31000		(Q) = 0.
63347	75	10100	03351		Subtract -5 from (Q)
63350	23	31000	07601		100 times. (Q) = +500.
63351	22	00036	32000	r23e	(A) = +5.
63352	43	00024	03354		Compare (A) with (00024).
63353	14	12747	02045		Failed; Jump to error type-out.
63354	75	10050	03356		(07602) thru (07651)
63355	11	00020	07602		= +1.
63356	75	30043	03360		Modify constants by
63357	54	07603	00001		succeeding powers of 2.
63360	11	00020	31000		(Q) = +1.
63361	75	10044	03363	r27a	
63362	27	31000	07602		Build up -1 in (Q).
63363	21	31000	00020		Add +1 to (Q). (Q) = 0.
63364	47	03365	03366		Check (A) for 0.
63365	14	12747	23045		Failed; Jump to error type-out.
63366	31	00117	00001		$(A_L) = +1$, $(A_R) = 0$.
63367	32	00020	00000		$(A_L) = +1$, $(A_R) = +1$.
63370	75	10044	03372		
63371	27	32000	07602		Build -1 in (A_R).
63372	35	00021	32000	r27b	$(A_R) = +1$, $(A_L) = +1$.
63373	22	00000	32000		Transmit (A_L) to (A).
63374	43	00021	03376		Compare (A) with (00021).
63375	14	12747	22345		Failed; Jump to error type-out.
63376	11	00202	31000		Q = -0.
63377	31	00117	00001		$(A_L) = +1$, $(A_R) = 0$.
63400	75	20044	03402		Complement (07602)
63401	27	07602	31000	r27c	thru (07645).
63402	27	32000	07644		Modify A_R.
63403	22	00002	32000		(A) = +7.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
63404	43	00026	03406	Compare (A) with (00026).
63405	14	12747	21645	Failed; Jump to error type-out.
63406	31	00117	00001	$(A_L) = +1$, $(A_R) = 0$.
63407	75	00010	03411	
63410	27	32000	31000	Complement (A_R) 10 times.
63411	22	00000	32000	r27d (A) = +1.
63412	43	00020	03414	Compare (A) with (00020).
63413	14	12747	22245	Failed; Jump to error type-out.
63414	31	00117	00001	$(A_L) = +1$, $(A_R) = 0$.
63415	75	30043	03417	} Complement constants
63416	27	07603	07602	} 1 in succeeding bits.
63417	35	00020	32000	r27e $(A_L) = 2$, $(A_R) = 0$.
63420	22	00000	32000	(A) = +2.
63421	43	00021	03423	Compare (A) with (00021).
63422	14	12747	22045	Failed; Jump to error type-out.
63423	75	30200	03425	} Clear addresses
63424	27	07600	07600	} (07600) thru (07777).
63425	75	10200	03427	
63426	21	32000	07600	r27f } Add 0 to (A) 200 times.
63427	47	03430	03431	Check (A) = 0.
63430	14	12747	22645	Failed; Jump to error type-out.
63431	11	00020	31000	Q = +1.
63432	75	10152	03434	} Add (Q) to (A) and shift by
63433	31	31000	00001	r31a } increasing amounts.
63434	43	00074	03436	Compare (A) with (00074).
63435	14	12705	23045	Failed; Jump to error type-out.
63436	11	00026	32000	(A) = +7.
63437	75	10011	03441	} Shift (A) by increasing
63440	31	32000	00001	r31b } amounts.
63441	47	03442	03443	Check (A) = 0.
63442	14	12705	22345	Failed; Jump to error type-out.
63443	75	10176	03445	} (07601) thru (07776)
63444	11	00020	07601	} = +1.
63445	75	30152	03447	} Add +1 to (A) and shift
63446	31	07601	00001	r31c } by increasing amounts.
63447	43	00074	03451	Compare (A) with (00074).
63450	14	12705	21645	Failed; Jump to error type-out.
63451	11	00203	32000	(A) = 0.
63452	11	00020	31000	(Q) = +1.
63453	75	00110	03455	
63454	32	31000	00001	r32a } Form "1"'s in all bits of (A).
63455	43	00202	03457	Compare (A) with (00202).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
63456	14	12707	43045	Failed; Jump to error type-out.
63457	31	00117	00001	$(A_L) = +1$, $(A_R) = 0$.
63460	35	00020	32000	$(A_L) = +1$, $(A_R) = +1$.
63461	75	00066	03463	} Add (A_R) to (A_R) and shift
63462	32	32000	00001	r32b } (A) by one place.
63463	22	00000	32000	$(A_L) = +1 = (A)$.
63464	43	00020	03466	Compare (A) with (00020).
63465	14	12707	42345	Failed; Jump to error type-out.
63466	11	00203	32000	(A) = 0.
63467	75	20110	03471	}
63470	32	07601	00001	r32c } Build all "1"'s in (A).
63471	43	00202	03473	Compare (A) with (00202).
63472	14	12707	41645	Failed; Jump to error type-out.
63473	11	00203	32000	(A) = 0.
63474	75	20110	03476	} Repeatedly subtract 1
63475	33	07601	00110	} from (A) and shift 110 times.
63476	21	32000	00020	r33a Add 1 to (A), (A) = 0.
63477	47	03500	03501	Check (A) = 0.
63500	14	12707	03045	Failed; Jump to error type-out.
63501	11	00026	31000	(Q) = +7.
63502	75	10011	03504	} Subtract +7 from (A) and
63503	33	31000	00100	} shift by increasing amounts.
63504	21	32000	31000	r33b Add (Q) to (A).
63505	47	03506	03507	Check (A) = 0.
63506	14	12707	02345	Failed; Jump to error type-out.
63507	11	00020	32000	(A) = +1.
63510	75	10003	03512	} Subtract (A) from zero
63511	33	32000	00001	r33c } and shift by increasing amounts.
63512	43	00163	03514	Compare (A) with (00163).
63513	14	12707	01645	Failed; Jump to error type-out.
63514	11	00021	32000	(A) = +2.
63515	75	20175	03517	} Subtract 1 from (A) and
63516	34	07601	00001	r34a } shift (A) left one. Repeat 175 times.
63517	43	00021	03521	Compare (A) with (00021).
63520	14	12706	43045	Failed; Jump to error type-out.
63521	11	00201	32000	(A) = -1.
63522	75	00044	03524	} Split subtract (A_R) from
63523	34	32000	00001	r34b } (A) and shift (A) one.
63524	43	00020	03526	Compare (A) with (00020).
63525	14	12706	42345	Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
63526	11	00020	31000	(Q) = +1.
63527	11	00021	32000	(A) = +2.
63530	75	07777	03532	r34c } Subtract 1 from 2 then shift
63531	34	31000	00001	it back to 2. Repeat.
63532	43	00021	03534	Compare (A) with (00021).
63533	14	12706	41645	Failed; Jump to error type-out.
63534	75	10050	03536	} (07600) thru (07647)
63535	11	00026	07600	} = +7.
63536	54	07600	00040	(07600) = 34 00000 00000.
63537	11	00026	32000	(A) = +7.
63540	75	30040	03542	r35a } Starting with +7, double
63541	35	07601	07602	(A) 40 times.
63542	43	07600	03544	Compare (A).
63543	14	12706	23045	Failed; Jump to error type-out.
63544	75	30040	03546	} Starting with +7, subtract
63545	36	07601	07701	} doubled constants from (A).
63546	11	07740	32000	r36a (A) = +7.
63547	43	07601	03551	Compare (A) with (07601).
63550	14	12706	63045	Failed; Jump to error type-out.
63551	11	00024	07600	(07600) = +5.
63552	54	07600	00040	(07600) = 24 00000 00000.
63553	11	00024	32000	(A) = +5.
63554	75	10040	03556	} Starting with +5, double
63555	35	32000	07700	r35b } (A) 40 times.
63556	23	07600	07737	Clear (A) if test works.
63557	47	03560	03561	Check (A) = 0.
63560	14	12706	22345	Failed; Jump to error type-out.
63561	11	00024	31000	(Q) = +5.
63562	75	10101	03564	} Effectively starting with +5 and
63563	35	31000	07601	} doubling (Q) 100 times (exceeds modulus).
63564	11	07701	32000	r35c (A) = Final result of previous operation.
63565	43	00055	03567	Compare (A) with constant.
63566	14	12706	21645	Failed; Jump to error type-out.
63567	11	00026	31000	Q = +7.
63570	31	00026	00006	A = +700.
63571	75	10077	03573	} Subtract +7 from (A)
63572	36	31000	07700	r36b } 77 times.
63573	11	07776	32000	(A) = result of previous step.
63574	43	00026	03576	Compare (A) with constant.
63575	14	12706	62345	Failed; Jump to error type-out.
63576	75	10177	03600	} (07601) thru (07777)
63577	11	00020	07601	r36c } = +1.
63600	11	00040	07600	(07600) = +200.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
63601	31	00040	00001		A = +400.
63602	75	20177	03604		} Subtract 1 from (A) 1778
63603	36	07601	31000		} times. (Q) = 201.
63604	23	31000	07600	r36c	Subtract 200 from (Q).
63605	43	00020	03607		Compare (A) with Constant
63606	14	12706	61645		Failed; Jump to error type-out.
63607	11	00020	31000		Q = +1.
63610	31	00117	00002		(A_L) = +2, (A_R) = 0.
63611	75	00003	03613		
63612	36	31000	31000		Subtract (Q) from (A).
63613	35	00020	31000	r36d	Add 1 to (A).
63614	22	00000	32000		(A_L) to (A_R). (A) = +2.
63615	43	00021	03617		Compare (A) with constant.
63616	14	12706	62245		Failed; Jump to error type-out.
63617	11	00064	32000		(A) = 00 40000 00000.
63620	75	10200	03622		} (07600) thru (07777)
63621	11	32000	07600		} = 00 40000 00000.
63622	75	20177	03624		} Sum of 200 addresses
63623	35	07600	32000	r35d	} in (A). Exceeds modulus.
63624	22	00000	32000		(A_L) to (A_R). (A) = +1.
63625	43	00020	03627		Compare (A) with constant.
63626	14	12706	22245		Failed; Jump to error type-out.
63627	23	31000	31000		Clear Q. (Q) = 0.
63630	75	20200	03632		} Sum of 200 addresses to
63631	35	07600	31000		} Q. Exeeeding modulus.
63632	11	31000	32000	r35e	(A) = (Q) = 0.
63633	47	03634	03635		Check A for zero.
63634	14	12706	22045		Failed; Jump to error type-out.
63635	11	00020	32000		Set A to +1.
63636	75	00044	03640		} Double (A) 44 times
63637	35	32000	31000		} (A_R) to (Q).
63640	22	00000	32000	r35f	(A_R) to (A).
63641	21	32000	31000		(Q) plus (A) = (A).
63642	43	00020	03644		Compare (A) with constant.
63643	14	12706	22645		Failed; Jump to error type-out.
63644	11	00203	32000		(A) = 0.
63645	11	00074	31000		(Q) = 20 00000 00000.
63646	75	07777	03647		}
63647	35	31000	32000	r35g	} Double (Q) 74 times.
63650	22	00004	32000		Shift (A) 4 places, (A_L) to (A).
63651	43	00060	03653		Compare (A) with constant.
63652	14	12706	21345		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
63653	11	00203	32000	(A) = 0.
63654	11	00020	31000	(Q) = +1.
63655	75	00045	03657	r35h } Double (Q) 45 times.
63656	35	31000	31000	
63657	43	00020	03661	Compare (A) with constant.
63660	14	12706	20545	Failed; Jump to error type-out.
63661	75	10176	03663	} (07601) thru (07776)
63662	11	00026	07601	} = +7.
63663	11	00027	07641	(07641) = +12.
63664	11	00026	32000	(A) = +7.
63665	75	20041	03670	r42a } Repeated search for
63666	42	07601	03667	} larger number.
63667	31	31000	00001	JN-R to (A). Left shift one.
63670	43	00060	03672	Compare (A) with constant.
63671	14	12647	43045	Failed; Jump to error type-out.
63672	11	00027	32000	(A) = +12.
63673	75	20041	03676	} Search for number equal
63674	43	07601	03675	} to (A).
63675	31	31000	00001	r43a JN-R to (A). Left shift one.
63676	43	00060	03700	Compare (A) with constant.
63677	14	12647	03045	Failed; Jump to error type-out.
63700	11	00144	03706	(03706) = 75 20041 03716.
63701	11	00124	03707	(03707) = 42 07601 03710.
63702	11	00203	07600	(07600) = 0.
63703	15	03706	07600	(07600) = 00 00000 03716.
63704	11	00026	32000	(A) = +7.
63705	36	00020	07641	(A) = +6 = (07641).
63706	00	00000	00000	} Repeated search for
63707	00	00000	00000	} larger number. Jump out changed.
63710	55	31000	00017	(Q) = JN-R. Left shift 17.
63711	15	31000	03706	(03706) = v portion of (Q).
63712	23	07600	31000	r42b $(07600)_f = (07600)_i - (Q)$.
63713	21	03707	07600	$(03707)_f = (03707)_i + (07600)$.
63714	11	31000	07600	(07600) = (Q).
63715	45	00000	03704	(03704) = NI.
63716	23	31000	00061	$(Q)_f = (Q)_i - (00061)$.
63717	54	31000	00001	(Q) left shifted one in A.
63720	43	00064	03722	Compare (A) with constant.
63721	14	12647	42345	Failed; Jump to error type-out.
63722	11	00145	03727	} Instructions used to
63723	11	00125	03730	} set up the following
63724	11	00203	07600	} program by constants
63725	15	03727	07600	r43b } contained in text.
63726	11	00026	32000	(A) = +7.
63727	00	00000	00000	Repeated equality jump.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
63730	00	00000	00000		Jump out modified by program.
63731	55	31000	00017		(Q) = JN-R Left shifted 17.
63732	15	31000	03727		Modify w portion of repeat.
63733	23	07600	31000		Subtract (Q) from (07600).
63734	21	03730	07600		Modify jump-out of equality jump.
63735	11	31000	07600	r43b	(Q) to (07600).
63736	45	00000	03726		Jump to re-run program.
63737	23	31000	00061		Subtract (00061) from (Q).
63740	54	31000	00001		(Q) left shifted in A.
63741	43	00064	03743		Compare (A) with constant.
63742	14	12647	02345		Failed; Jump to error type-out.
63743	75	10200	03745		} (07600) thru (07777)
63744	11	00064	07600		} = 00 40000 00000.
63745	11	00026	07601		(07601) = +7.
63746	11	00202	31000		(Q) = All "7"'s.
63747	75	30176	03751	r51	} Transmit +7 to previous
63750	51	07601	07602		} addresses thru "1"'s mask in Q.
63751	11	07601	32000		(A) = +7.
63752	43	07776	03754		Compare (A) with final result.
63753	14	12625	24500		Failed; Jump to error type-out.
63754	11	00020	31000		(Q) = +1.
63755	11	31000	32000		(A) = +1.
63756	75	20004	03760		} (Q) = result of repeated
63757	52	07601	31000		} (A) + L(Q) (u).
63760	55	31000	00042	r52a	(Q) shifted 42.
63761	35	31000	32000		Add (Q) to (A).
63762	43	00027	03764		Compare (A) with constant.
63763	14	12627	43045		Failed; Jump to error type-out.
63764	23	31000	31000		Clear Q & A. (Q) = 0. (A) = 0.
63765	75	30175	03767		} (07601) thru (07775)
63766	52	07602	07601		} = (A) + L(Q) (u) = 0.
63767	75	20175	03771	r52b	} Sum of addresses
63770	35	07601	32000		} (07601) thru (07775) in A.
63771	43	31000	03773		Compare (A) with (Q).
63772	14	12627	42345		Failed; Jump to error type-out.
63773	31	00064	00003		(A_R) = 04 00000 00000. (A_L) = 0.
63774	11	32000	07600		(07600) = (A_R).
63775	11	00020	31000		(Q) = +1.
63776	11	31000	32000		(A) = +1.
63777	75	00040	04001	r52c	} Double (Q) 40 times.
64000	52	31000	31000		}
64001	43	07600	04003		Compare (A) with constant.
64002	14	12627	41645		Failed; Jump to error type-out.
64003	11	00116	32000	r52d	(A_R) = 37 77777 77762.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v		FUNCTION
64004	35	00031	31000		$(A)_f = (Q) = (A_R)_i + 15.$
64005	31	00066	00002		(A_R) = 04 00000 00000.
64006	11	32000	07600		(07600) = 04 00000 00000.
64007	11	00020	32000		(A) = +1.
64010	75	00040	04012	r52d	Effect of doubling (A)
64011	52	32000	32000		thru mask in Q 40 times.
64012	43	07600	04014		Compare (A) with known value.
64013	14	12627	42245		Failed; Jump to error type-out.
64014	31	00117	00000		(A) = 40 00000 00000.
64015	11	00020	31000		(Q) = +1.
64016	75	00044	04020		Subtract 44 from (A)
64017	36	31000	32000		
64020	11	00202	31000		(Q) = all "7"'s.
64021	22	10000	32000		Clear A_L. (A_R) to A.
64022	54	32000	00044		Shift (A) 44 places.
64023	52	31000	32000	r52e	(A) + L(Q) (Q) to A.
64024	75	10044	04026		(A) + L(Q) (A) = (07601) thru (07644).
64025	52	32000	07601		
64026	35	07644	32000		(A) + (07644).
64027	22	10001	32000		Shift A one. Clear (A_L). (A_R) to A.
64030	43	00020	04032		Compare (A) with constant.
64031	14	12627	42045		Failed; Jump to error type-out.
64032	11	00020	31000		(Q) = +1.
64033	31	00117	00001		(A_L) = +1. (A_R) = 0.
64034	35	31000	32000		(A_L) = +1. (A_R) = +1.
64035	75	00044	04037		
64036	52	32000	31000	r52f	(A) + L(Q) (A) 44 times to A.
64037	22	00000	32000		$(A) = (A_L)_i$
64040	21	32000	31000		Add (Q) to (A).
64041	43	00021	04043		Compare (A) with constant.
64042	14	12627	42645		Failed; Jump to error type-out.
64043	11	00026	07601		(07601) = +7.
64044	53	31000	31000		(Q) = All "1"'s.
64045	75	30176	04047		(07601) thru (07602)
64046	53	07601	07602	r53a	= +7.
64047	43	07601	04051		Compare (A) with known value.
64050	14	12627	03045		Failed; Jump to error type-out.
64051	11	00203	32000		Clear A. (A) = 0.
64052	11	00020	31000		(Q) = +1.
64053	75	10175	04055		(07602) thru (07776)
64054	53	32000	07602	r53b	= +6.
64055	11	07776	32000		(A) = (07776).
64056	43	00025	04060		Compare (A) with constant.
64057	14	12627	02345		Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
64060	11	07775	07776	(07776) = (07775) = +6.
64061	75	10175	04063	} (07602) thru (07776)
64062	53	31000	07602	} = +7.
64063	23	07776	00026	r53c (07776) = 0 = (A).
64064	35	31000	32000	Add (Q) to A. (A) = +1.
64065	43	00020	04067	Compare (A) with constant.
64066	14	12627	01645	Failed; Jump to error type-out.
64067	53	31000	31000	(Q) = All ones.
64070	11	00024	32000	(A) = +5.
64071	75	00100	04073	} Same operation 100 times
64072	53	32000	32000	r53d } (A) = +5 each time.
64073	43	00024	04075	Check (A) with constant.
64074	14	12627	02245	Failed; Jump to error type-out.
64075	51	31000	32000	(Q) = (A_R) = All ones.
64076	75	00100	04100	} Same operation
64077	53	32000	31000	} (A_R) = All ones.
64100	35	00020	32000	r53e Add +1 to (A).
64101	22	00000	32000	(A_L) to (A) = +1.
64102	43	00020	04104	Compare (A) with constant.
64103	14	12627	02045	Failed; Jump to error type-out.
64104	11	00026	32000	(A) = +7.
64105	75	10176	04107	}
64106	11	32000	07601	} (07601) thru (07775) = +7.
64107	75	20175	04111	r53f } Operation performed on
64110	53	07601	31000	} addresses (07601) thru (07775) = +7.
64111	43	00026	04113	Check (A) with constant.
64112	14	12627	02645	Failed; Jump to error type-out.
64113	11	00203	31000	Clear Q.
64114	75	00002	04116	
64115	53	31000	31000	(A_R) = (Q) = All "1"'s.
64116	52	31000	32000	(A) = $(A)_i$ + L(Q) (Q).
64117	35	00021	32000	r53g Add +2 to (A).
64120	22	00000	32000	(A_L) to (A).
64121	43	00021	04123	Compare (A) with constant.
64122	14	12627	01345	Failed; Jump to error type-out.
64123	75	30135	04125	} (07601) thru (07735)
64124	54	07601	00001	} shifted by increasing increments of one.
64125	43	07625	04127	r54a Compare (A) with test word.
64126	14	12626	43045	Failed; Jump to error type-out.
64127	11	00026	32000	(A) = +7.
64130	75	10014	04132	}
64131	54	32000	00001	r54b } Shift (A) by increasing amounts up to 14.
64132	43	07716	04134	Compare (A) with known value.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
64133	14	12626	42345	Failed; Jump to error type-out.
64134	11	00024	31000	(Q) = +5.
64135	75	10010	04137	} Shift (Q) by increasing
64136	54	31000	00001	} amounts up to 10.
64137	22	00000	32000	r54c (A_L) to (A).
64140	32	31000	00000	Split add (Q) to A.
64141	43	00024	04143	Compare (A) with constant.
64142	14	12626	41645	Failed; Jump to error type-out.
64143	11	00174	31000	(Q) = -6.
64144	75	10024	04146	} Shift (Q) by increasing
64145	55	31000	00001	} amounts up to 24.
64146	11	31000	32000	r55a (Q) = (A).
64147	43	00141	04151	Compare (A) with constant.
64150	14	12626	23045	Failed; Jump to error type-out.
64151	11	00026	32000	(A) = +7.
64152	75	10011	04154	} Shift (A) in Q by increasing
64153	55	32000	00001	} amounts up to 11.
64154	21	32000	00154	r55b Subtract constant from (A).
64155	47	04156	04157	Check (A) for zero.
64156	14	12626	22345	Failed; Jump to error type-out.
64157	75	10200	04161	} (07600) thru (07777)
64160	11	00105	07600	} = 35 61414 31313.
64161	75	20200	04163	} (07600) thru (07777)
64162	55	07600	00044	r55c } shifted in Q by 44.
64163	11	00105	32000	(A) = (00105).
64164	43	07600	04166	Compare (A) with first shifted word.
64165	14	12626	21645	Failed; Jump to error type-out.
64166	43	07776	04170	Compare (A) with last shifted word
64167	14	12626	22245	r55d Failed; Jump to error type-out.
64170	75	10177	04172	} (07601) thru (07777)
64171	11	00024	07601	} = +5.
64172	11	00024	32000	(A) = +5.
64173	75	10014	04175	} Build up (A) by multiples
64174	71	32000	07601	r71a } of +5, 14 times.
64175	75	20014	04177	} Divide (A) by +5, 14
64176	73	07601	32000	} times.
64177	43	07615	04201	Compare (A) with +5.
64200	14	12725	23045	Failed; Jump to error type-out.
64201	75	30175	04203	} Multiply +5 times +5
64202	71	07601	07602	} 175 times (A) = +31.
64203	73	07776	31000	r71b Divide (A) by +5.
64204	47	04205	04206	Check remainder for zero.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
64205	14	12725	22345	Failed; Jump to error type-out.
64206	11	31000	32000	Quotient to A.
64207	43	07601	04211	r71c Check quotient for +5.
64210	14	12725	21645	Failed; Jump to error type-out.
64211	75	20175	04213	} Multiply +5 times +5
64212	71	07601	31000	} 175 times (A) = +31.
64213	73	07601	31000	r71d Divide (A) by +5.
64214	47	04215	04216	Check remainder for zero.
64215	14	12725	22245	Failed; Jump to error type-out.
64216	11	31000	32000	Quotient to A.
64217	43	07775	04221	r71e Check quotient with +5.
64220	14	12725	22045	Failed; Jump to error type-out.
64221	11	00020	32000	(A) = +1.
64222	75	00100	04224	} Multiply (A) by (A)
64223	71	32000	32000	r71f } 100 times.
64224	43	31000	04226	Compare (A) and (Q).
64225	14	12725	22645	Failed; Jump to error type-out.
64226	11	07601	31000	(Q) = +5.
64227	75	00100	04231	} Multiply (Q) by (Q)
64230	71	31000	31000	} 100 times.
64231	73	07601	31000	r71g Divide (A) by +5.
64232	47	04233	04234	Check remainder for zero.
64233	14	12725	21345	Failed; Jump to error type-out.
64234	11	31000	32000	Put quotient in A.
64235	43	07601	04237	r71h Check quotient for +5.
64236	14	12725	20545	Failed; Jump to error type-out.
64237	75	20100	04241	} Multiply +5 by 0
64240	71	07601	32000	} 100 times.
64241	47	04242	04243	r71i Check (A) for zero.
64242	14	12725	21445	Failed; Jump to error type-out.
64243	75	00100	04245	} Multiply +5 by 0
64244	71	31000	32000	} 100 times.
64245	47	04246	04247	r71j Check (A) for zero.
64246	14	12725	23245	Failed; Jump to error type-out.
64247	75	00100	04251	} Multiply 0 by 0
64250	71	32000	32000	} 100 times.
64251	47	04252	04253	r71k Check (A) for zero.
64252	14	12725	23645	Failed; Jump to error type-out.

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
64253	11	00026	31000	(Q) = +7.
64254	11	31000	32000	(A) = +7.
64255	75	10176	04257	} (07601) thru (07776)
64256	11	00026	07601	} = +7.
64257	75	00077	04261	} Starting with +7
64260	35	31000	32000	} add +7 to (A) 778 times.
64261	11	32000	07600	r72a (07600) = (A).
64262	11	00203	32000	(A) = 0.
64263	11	00020	31000	(Q) = +1.
64264	75	10100	04266	} (A) plus 1 times 7
64265	72	31000	07601	} 100 times.
64266	43	07600	04270	Check (A) with known word.
64267	14	12727	43045	Failed; Jump to error type-out.
64270	11	00203	32000	Clear A.
64271	75	30100	04273	} $(A)_f$ = 100 times 7 times 7.
64272	72	07601	07602	
64273	73	07600	31000	r72b Divide (A) by 100 times +7.
64274	47	04275	04276	Check remainder for zero.
64275	14	12727	42345	Failed; Jump to error type-out.
64276	11	31000	32000	Put quotient in A.
64277	43	07701	04301	r72c Check quotient with +7.
64300	14	12727	41645	Failed; Jump to error type-out.
64301	11	00020	32000	(A) = +1.
64302	75	10013	04304	} $(A)_f = 8^{13}$.
64303	72	32000	07601	
64304	36	31000	32000	r72d Subtract 8^{12} from (A).
64305	73	31000	31000	Divide 7 times 8^{12} by 8^{12}.
64306	47	04307	04310	Check remainder for zero.
64307	14	12727	42245	Failed; Jump to error type-out.
64310	11	31000	32000	Put quotient in A.
64311	43	07601	04313	r72e Check quotient for +7.
64312	14	12727	42045	Failed; Jump to error type-out.
64313	31	00117	00001	(A_L) = +1, (A_R) = 0.
64314	35	00020	32000	(A_L) = +1, (A_R) = +1.
64315	75	00044	04317	} Repeated multiply add, building
64316	72	32000	32000	} up word in A.
64317	36	00020	32000	r72f Subtract one from (A).
64320	22	00000	32000	(A_L) to (A).
64321	43	00020	04323	Check (A) for +1.
64322	14	12727	42645	Failed; Jump to error type-out.
64323	11	00066	31000	(Q) = 01 00000 00000.
64324	31	00117	00001	r72g (A_L) = +1, (A_R) = 0.
64325	75	00100	04327	(A) plus (Q) by (A).

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TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
64326	72	31000	32000	100 times.
64327	22	00000	32000	(A_L) to (A).
64330	43	00021	04332	r72g Check (A) for +2.
64331	14	12727	41345	Failed; Jump to error type-out.
64332	31	00117	00002	$(A_L) = +2$, $(A_R) = 0$.
64333	75	20040	04335	} $(A)_i$ + 7 times $(A)_i = (A)_f$.
64334	72	07601	32000	}
64335	36	07600	32000	r72h Subtract (07600) from (A).
64336	22	00000	32000	(A_L) to (A).
64337	43	00021	04341	Check (A) with +2.
64340	14	12727	40545	Failed; Jump to error type-out.
64341	11	00203	32000	Clear A.
64342	75	20100	04344	} $(A)_f = (A)_i$ + 7 times 7
64343	72	07601	31000	} 100 times.
64344	73	07600	31000	r72i Divide (A) by (07600).
64345	47	04346	04347	Check remainder for zero.
64346	14	12727	41445	Failed; Jump to error type-out.
64347	11	31000	32000	Put quotient in (A).
64350	43	07601	04352	r72j Check quotient with +7.
64351	14	12727	43245	Failed; Jump to error type-out.
64352	11	00020	32000	(A) = +1.
64353	75	00004	04355	} 1 + 1·1, 2 + 2·2, 6 + 6·6 ...
64354	72	32000	31000	} etc. 4 times.
64355	11	32000	00207	(00207) = (A).
64356	75	00002	04360	} Continuation of previous
64357	72	32000	31000	r72k } sequence.
64360	73	00207	31000	Divide (A) by (00207).
64361	35	31000	32000	Subtract quotient from (A).
64362	36	00070	32000	Add (00070) to (A).
64363	47	04364	04365	Check (A) for zero.
64364	14	12727	43645	Failed; Jump to error type-out.
64365	11	00201	32000	(A) = -1.
64366	75	00003	04370	}
64367	72	32000	31000	r72L } $(A)_i + (A)_i$ times (Q) = $(A)_f$.
64370	47	04371	04372	Check (A) for zero.
64371	14	12727	41145	Failed; Jump to error type-out.
64372	11	07601	31000	(Q) = +7.
64373	11	00203	32000	(A) = 0.
64374	75	00100	04376	} $(A)_f = (A)_i$ + 7 times 7
64375	72	31000	31000	r72m } 100 times.
64376	73	07600	32000	Divide (A) by (07600).
64377	43	07601	04401	Check (A) with +7.
64400	14	12727	40745	Failed; Jump to error type-out.

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
64401	75	10176	04403	} (07601) thru (07776)
64402	11	00026	07601	} = +7.
64403	11	00026	32000	(A) = +7.
64404	75	20040	04406	} 7 times 7 times 7, 40 times
64405	71	32000	07601	r73 } exceeds modulus.
64406	75	20014	04410	}
64407	73	07601	32000	} (A) divided by+7, 14 times.
64410	43	00020	04412	Compare (A) with +1.
64411	14	12727	04500	Failed; Jump to error type-out.
64412	11	00020	32000	(A) = +1.
64413	75	10077	04415	(07601) = 46. (07602) thru
64414	74	32000	07601	} (07677) = 0.
64415	11	00203	32000	} Clear A.
64416	75	20077	04420	
64417	35	07601	32000	r74a } Sum of 77 K in (A).
64420	75	00045	04422	
64421	36	00020	32000	} Subtract 45 "1"'s from (A).
64422	43	00020	04424	Compare (A) with +1.
64423	14	12726	43045	Failed; Jump to error type-out.
64424	11	00024	31000	(Q) = +5.
64425	75	10100	04427	} Scale (Q) 100 times
64426	74	31000	07601	} K in (07601) thru (07700).
64427	54	31000	00011	Shift (Q) in A 11 places.
64430	75	20100	04432	r74b } Subtract 50 from (A)
64431	36	07601	32000	} 100 times.
64432	47	04433	04434	Check (A) for zero.
64433	14	12726	42345	Failed; Jump to error type-out.
64434	11	00020	07601	(07601) = +1.
64435	75	30100	04437	} Scale (07601) put K in (07602)
64436	74	07601	07602	} Scale (07602) put K in (07603) etc.
64437	11	07701	32000	r74c (A) = (07701) = Last value of K
64440	43	07700	04442	Compare (A) with (07700).
64441	14	12726	41645	
64442	56	20000	04443	Stop, if selected.
64443	45	30000	00210	Repeat QUAK, if selected.
64444	75	30020	00050	
64445	11	64446	00050	
64446	75	30003	00052	
64447	11	46700	00100	Block transfer and modify
64450	13	00065	31050	short command test.
64451	75	30024	00055	
64452	51	46703	00103	

TABLE 1. QUAK TEST (Cont.)

ADDRESS	OP-CODE	u	v	FUNCTION
64453	11	00062	00106	
64454	11	00063	00111	
64455	16	00064	00101	
64456	61	00000	00052	
64457	45	00000	00100	
64460	45	00000	64464	
64461	11	00106	01661	Constants.
64462	00	00000	00110	
64463	00	46600	00000	
64464	75	34466	00210	Reload QUAK in cores.
64465	11	60001	00001	
64466	11	60000	00000	Set jump in F_1.
64467	75	34477	04471	
64470	11	60001	00001	Block transfer QUAK.
64471	14	45473	53430	Print -QUAK-
64472	14	36570	40000	
64473	45	30000	00210	Jump to run QUAK.
64474	14	56044	71503	
64475	14	03265	70404	Print -POOF-
64476	45	00000	00210	

MAINTENANCE SCHEDULES

1. GENERAL

The following maintenance schedules are provided as a general outline to follow in performing maintenance at each Univac Scientific installation. For specific information on performance of any part of the schedule, refer to the corresponding section in the maintenance manual or the particular external equipment manual. In performing scheduled maintenance keep in mind that the maintenance should be of a preventive nature as much as possible. Cleanliness of the equipment and the surrounding area is an important contributing factor to good maintenance.

2. DAILY MAINTENANCE SCHEDULE

1) Energize the computer.

2) Check water flow and water temperature in blower cabinet.

3) Check operating voltages and adjust same. Check again about one-half hour after equipment is energized.

4) Load maintenance routines on magnetic drum if necessary. (Maintenance routines should be stored on drum before turning off power to machine at the end of the day.)

5) Run Magnetic Core Test on high margins and low heaters, and on low margins in the magnetic core section.

6) Run long Command Test with low heaters on control, arithmetic, and magnetic drum sections.

7) Run Quack 15 times with low heaters on arithmetic, control, and magnetic drum sections.

8) Run tests on external equipment such as Controlled Card Reproducer, Magnetic Tape Units, and High-Speed Printer. See daily maintenance routines for equipment concerned. Clean Ferranti Reader mask and light source bulb while other tests are running.

9) Run High-Speed Punch and Tape Reader Tests. Read paper tape with alternately high and low margins.

Rotation of spare chassis should be accomplished daily after the tests concerning the intended chassis location have been completed. The tests concerning the chassis involved should be rerun on margins and low heaters for a check of the replacement chassis.

3. WEEKLY MAINTENANCE ON COMPUTERS

1) One turn to grease cups on blower shaft bearings.

2) Check alternator drive motor for cleanliness. Blow out with air hose if necessary.

3) Check motor bearings for overheat and noise.

4) Alternator commutator may need occasional wiping with dry canvas or nonlinting material. (It should maintain good polish.)

5) Check alternator for cleanliness.

6) Punch tape test with low heaters on drum, controls and arithmetic sections, and margins on reader.

7) Check marginal operation by varying all voltages during short Command Test and Quack. Note any tendency of operating voltage margins to narrow when compared with previous operating margins.

8) Run PCR Test with low heaters on magnetic drum, control, and arithmetic, and with margins on magnetic drum.

9) Check out repaired spare chassis which had been removed from the machine because of malfunctions during the week.

10) Run the five vdc down 40 percent, and see if any of the indicators on the Supervisory Control Panel set.

11) Run the five vdc up to top of meter, and see if any indicators on Supervisory Control Panel set.

12) Set all indicators manually on the panel and repeat steps 10 and 11.

13) Run Convair Drum Test on four interlace with control, arithmetic, and magnetic drum on low heaters.

14) Perform required periodic maintenance on external equipment.

15) General clean-up of the computer such as desks, floors, cabinets.

4. MONTHLY MAINTENANCE ON COMPUTERS

1) Check rundown time full speed to full stop on drum. (Decrease of 25 percent warrants notification to St. Paul.)

2) Perform monthly periodic maintenance on external equipment.

5. QUARTERLY MAINTENANCE ON COMPUTERS

    1) Air filter exchange (or when noticeable amount of dirt has accumulated).

    2) Check on motorized valve adjustment.

    3) Apply lubriplate to moving parts of motorized valve.

    4) Refill grease cups on blower shaft bearings.

6. ANNUAL COMPUTER MAINTENANCE

    1) Repacking of drum drive motor bearings.

    2) Remove grease cups on blower shaft bearings, clean bearings and grease cups, and refill grease cups.